World's most advanced Baseband IP platform for Mobile Broadband 5G

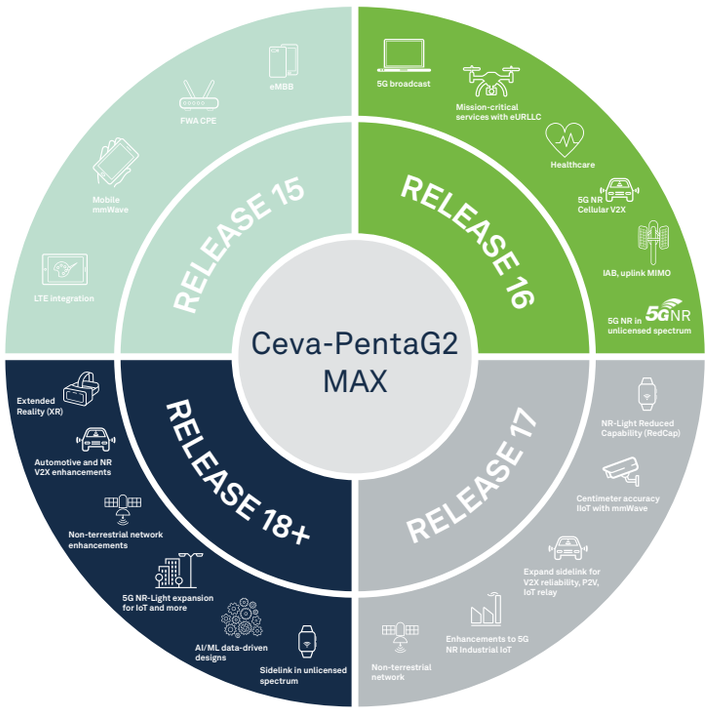
Ceva-PentaG2 Max is industry's most comprehensive IP Platform capable of meeting the extreme low latency, and strict power budget for 3GPP 5G UE broadband eMBB and URLLC devices

Key Benefits

- Fully configurable IP platform for 5G NR and legacy 4G multi-mode RAT, targeting both
- Scalable and customizable heterogeneous compute platform, with optimal HW/SW partitioning using a set of vector and scalar DSPs, co-processors and HW accelerators for achieving customer power and performance target

  Complete inline acceleration of all major processing chains for both downlink and uplink
- Optimized HW accelerators for FFT, Equalization, Bit/Symbol modulation and demodulation, MLD, and FEC
- Leveraging industry proven Ceva-XC4500 vector baseband DSP with 5G ISA extensions
- Reference end-to-end SW Implementation of major processing chains, Including PDSHC, PDCCH, PUSCH
- Comprehensive System-C SoC simulator, modeling all platform components, demonstrating major processing chains, allowing fast prototyping, proof of concept and solution dimensioning
- Second generation of PentaG architecture, reducing TTM, risk, effort and cost for new SoC development

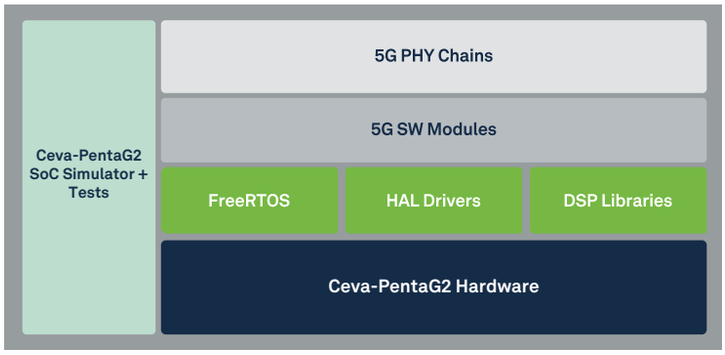
Ceva-PentaG2 - Target Applications Diagram



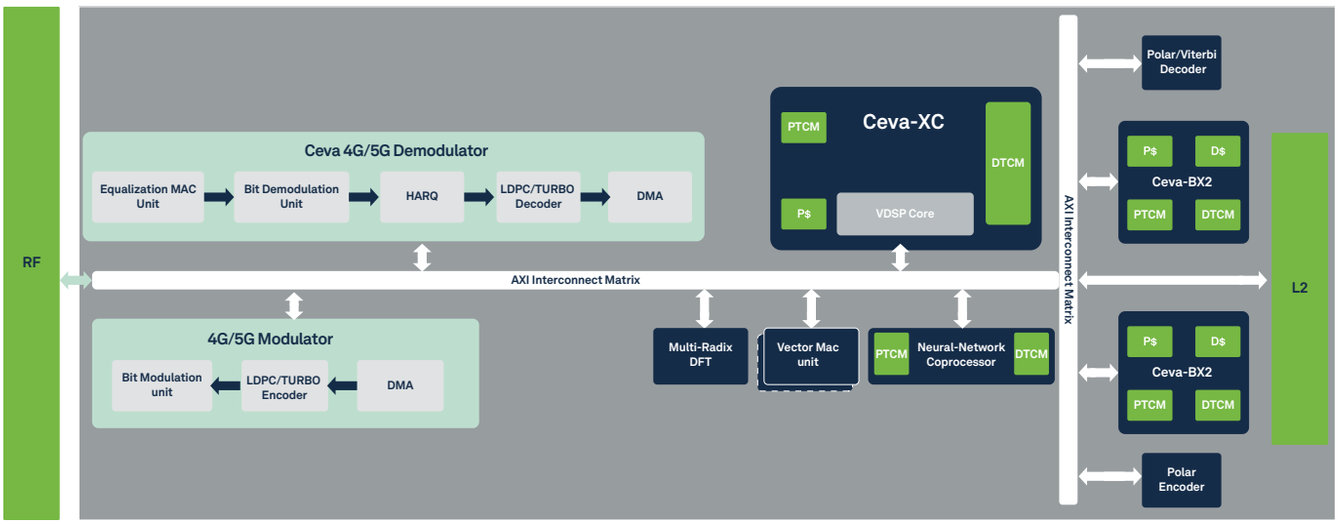
Applications and use-cases

- 5G-NR & LTE UE devices
  - Handsets and Cellular baseband
  - Notebook datacard
  - FWA (Fixed Wireless Access) and CPE
  - XR & Headsets
  - Mission Critical
  - C-V2X (Cellular V2X)
  - Repeaters and IAB

Ceva-PentaG2 MAX deliverables



Ceva-PentaG2 Max Block Diagram



The Key Aspects of PentaG2-Max

Enhanced Ceva-XC4500 DSP with 5G ISA Extensions	Field-proven DSP with new 5G ISA extensions specifically designed to accelerate key functions in the modem. Customer extendable using Ceva-Xtend
Ceva-BX2 scalar DSPs	Multiple Ceva-BX2 cores designed to address high performance and ultra-low latency demands of 5G PHY control.
Vector MAC Unit (VMU) Co-Processor	64 MAC co-processor designed to handle advanced channel estimation measurements and schemes in multiple channels.
TCEs and Accelerators	A set of HW accelerators, including FEC encoders/decoders, FFTs, MLD (LTE), etc.
NNCP AI Processor	Designed to handle advanced beamforming techniques and link adaptation scenarios using neural networks.
System-level Simulation	An integrated C-level simulation environment that allows system engineers, architects and SW developers to model, pro le and debug at cycle-accurate system level.
SW libraries and chains	A rich set of DSP, Comm and 5G libraries, as well as complete reference chains (e.g. PDCCH receiver)

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