Integrative baseband IP platform for Cellular IoT

PentaG2-Lite™ is industry's first comprehensive and integrative baseband IP Platform meeting challenging tight power envelope targets for next generation cellular IoT devices, supporting LTE Cat.1 and future 5G RedCap devices.

Key Benefits

- Lean and compact architecture, supporting reduced capacity use cases
- Supporting a range of BW configurations, from Rel 17 20MHz, to future Rel 18 5/10MHz, and 1 or 2 antennas option
- Complete acceleration of all major processing chains for both downlink and uplink, achieving extreme power consumption constraint targets
- Flexible and customizable baseband platform, with optimal HW/SW partitioning using a single scalar DSP controller and HW accelerators
- Optimized and efficient HW accelerators for FFT, Equalization, Bit/Symbol modulation and demodulation, and FEC
- Leveraging industry proven small footprint CEVA-BX2 as PHY controller DSP, able to run the protocol stack as well for tight Integration
- Reference end-to-end SW implementation of major processing chains, including PDSCH, PDCCH, PUSCH
- Comprehensive System-C SoC simulator, modeling all platform components, demonstrating major processing chains (HW+SW), allowing fast prototyping, proof of concept and solution dimensioning
- Second generation and scaled down version of PentaG architecture, reducing TTM, risk, effort and cost for new SoC development

Applications and use-cases

- 5G-NR & LTE UE low power devices
  - 5G RedCap (a.k.a. NR-Lite)
  - LTE Cat1 to Cat4
  - Wearables
  - Surveillance cameras
  - Industrial sensing
  - Car telemetry
  - M2M Modules
  - Asset tracking
  - Share bike

PentaG2 deliverables

- 5G PHY Chains
- 5G SW Modules
- FreeRTOS
- HAL Drivers
- DSP Libraries
- PentaG2 Hardware
The Key Aspects of PentaG2-Lite

| Optimized lean and compact Baseband Solution | Achieving aggressive power consumption and area targets for low cost battery powered IoT devices |
| Complete Acceleration of Major Processing Chains | End-to-end acceleration of downlink and uplink processing chains, for both LTE Cat.1 and future 5G RedCap, re-using the same platform |
| Scalable and Flexible | Highly flexible architecture, allowing customers to dimension their solution using PentaG2 Building blocks, with standard AXI/APB interfaces, and add their own IP and secret sauce |
| Rich Set of HW Accelerators | Covering all processing chain components, including FFT/IFFT, Equalization, Symbol/Bit Modulation and Demodulation, HARQ, and 4G/5G FEC Encoding and Decoding |
| Low footprint DSP controller | Using field proven CEVA-BX2 scalar DSP for tightly coupled PHY control and HW accelerator sequencing. Can be used for running Protocol Stack as well |
| End-to-end 5G Processing Chains SW and libraries | Standard compliant reference implementation of major processing chains, including PDSCH, PDCCH, PUSCH, augmented with rich set of optimized 5G libraries |
| Comprehensive SoC Simulator | Modeling all PentaG2-Lite accelerators and DSP core, allowing pre-silicon SW development fast prototyping, PoC and solution dimensioning |