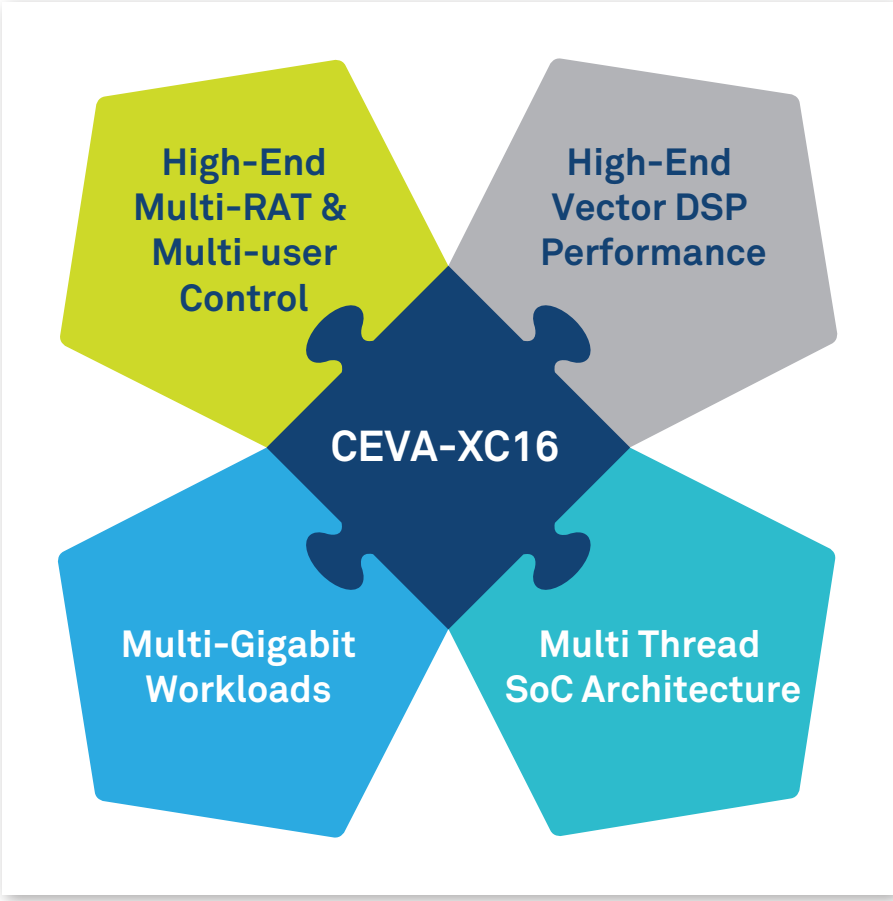
Enabling next generation 5G RAN - world's strongest vector DSP for cellular baseband applications

CEVA-XC16 is sixth generation vector processor IP from CEVA, designed to bring multi-gigabit high-end communication and cellular capabilities to base-stations, small-cells, gateways, access points and CPEs.

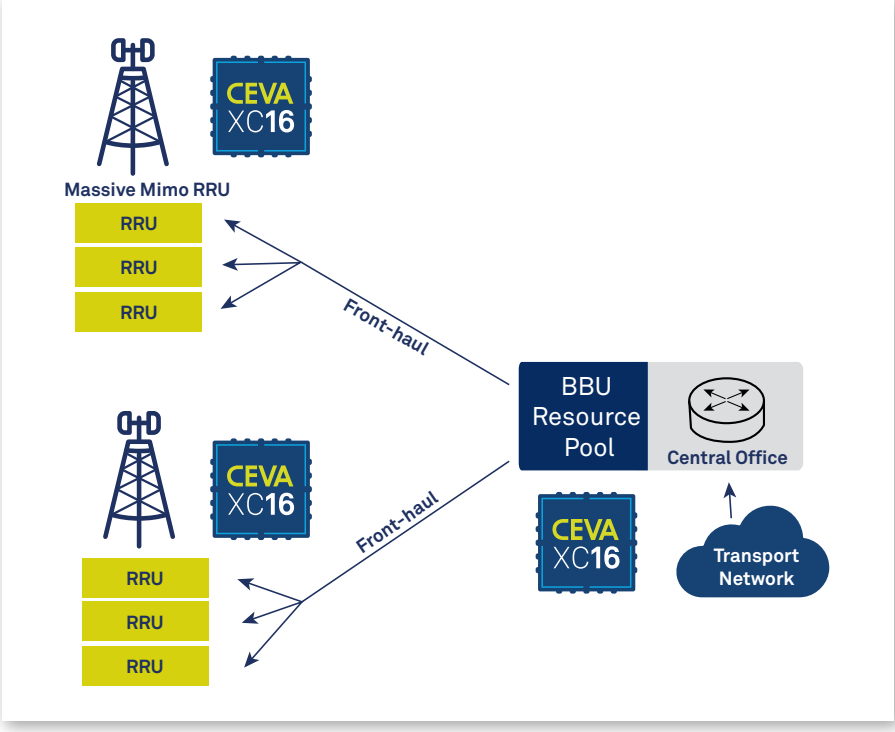


Key Benefits

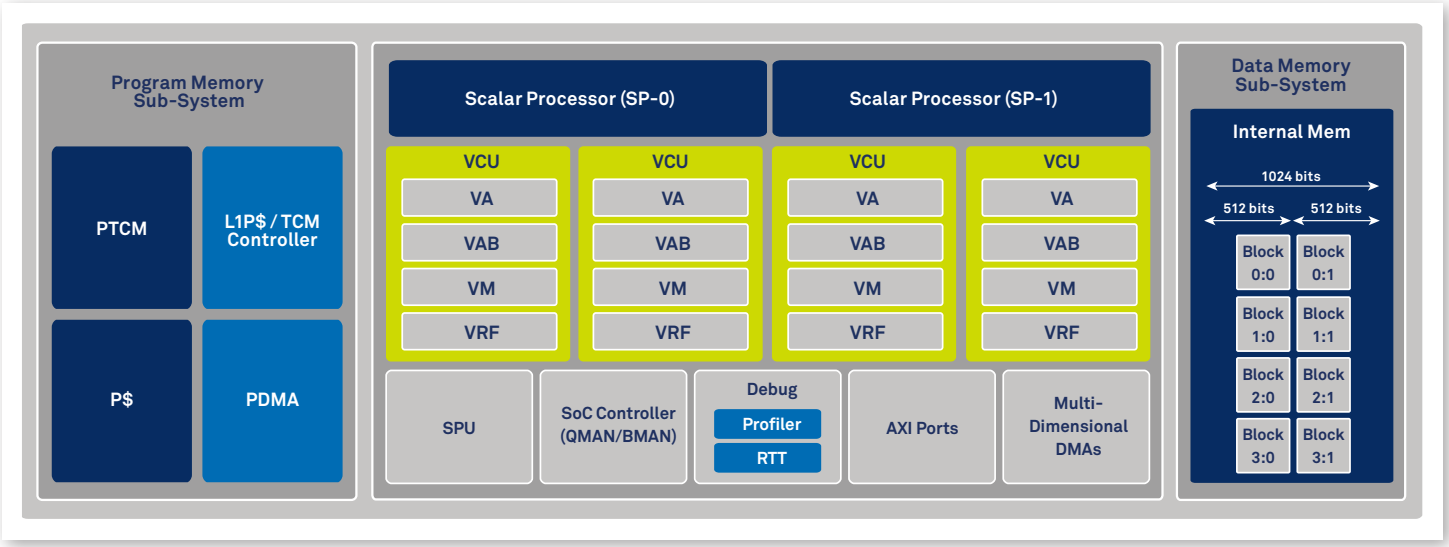
- **Meets the demanding requirements** of extreme multi-gigabit communications use cases and large-scale baseband aggregation
- **Scalable architecture** addresses the full range of eNodeB and gNB from femtocell, small cell, macrocell, BBU & RRH to Cloud-RAN
- **Quad-vector processor** addresses the needs of next-generation wireless applications such as 5G-NR, FWA, C-V2X, Wi-Fi 6 (802.11ax)
- **Dual-scalar processor** running simultaneous multi thread, third generation CEVA scalar architecture with superior code size
- **Enhanced Multi-User** capabilities, supporting dynamic massive single user and fine multi user allocations

Applications and use-cases

- **5G-NR & LTE-A Pro infrastructure**
  - Cloud-RAN, V-RAN, DU acceleration, BBU aggregation, Massive MIMO RRH, Massive Carrier Aggregation RRH, Macrocell, Small Cell, and IAB (Integrated Access and Back-haul), eCPRI compression and management
  - FWA (Fixed Wireless Access) and CPE
  - Supporting 3GPP Release 16 and 17 use cases, in both eMBB and uRLLC



CEVA-XC16 architecture diagram



Architecture Highlights

Core features

- Fully programmable DSP architecture incorporating unique mix of VLIW and SIMD vector capabilities
- Increased length pipeline enables unprecedented vector unit speeds, architected for advanced process nodes – up to 1.8GHz
- Best in class 2048-bit memory BW
- 8-way VLIW provides optimal hardware utilization
- Extremely powerful quad vector processor supports fixed- and floating-point operations with 256 MACs per cycle
- Dynamic allocation of vector units to scalar processors
- Unique high-precision arithmetic optimized for matrix processing up to 256x256 and for non-linear operators
- Fully redesigned third generation dual multi thread CPU/DSP SPU (Scalar Processing Unit) with optimizing C compiler for protocol, control, and DSP native C code
- SPU supports very low overhead RTOS multi-tasking with dynamic branch prediction
- Massive number of IoT/MTC users served by control plane

System features

- Core streaming interfaces support ultra-low latency
- AMBA 4 compliant matrix interconnect
- Comprehensive multicore support with ACE-compliant cache coherency
- Advanced high-bandwidth memory subsystem for efficient utilization of vector unit
- Hardware/software partitioning delivers exceptional power efficiency while maintaining software flexibility with Queue and Buffer Managers and AXI interfaces

USA (HQ)
1174 Castro Street
Suite 210
Mountain View
CA, 94040
Tel: +1 (650) 417 7900

Israel
2 Maskit Street
POBox 2068
Herzelia 46120
Tel: +972 9 961 3700

Ireland
18/19 South William Street, 2nd Floor
Dublin 2
Tel: +353 1 237 3900

France
RivieraWaves S.A.S
Les Bureaux Green Side 5, Bat 6
400, avenue Roumanille, 06410
Biot, Sophia Antipolis, France
Tel: +33 4 83 76 06 00

USA (East)
CEVA Technologies, Inc.
15245 Shady Grove Road
Suite 400
Rockville, MD 20850
Tel: +1 650 417 7900

For more information: