Enabling SDR based, very low power multi-gigabit mobile communications

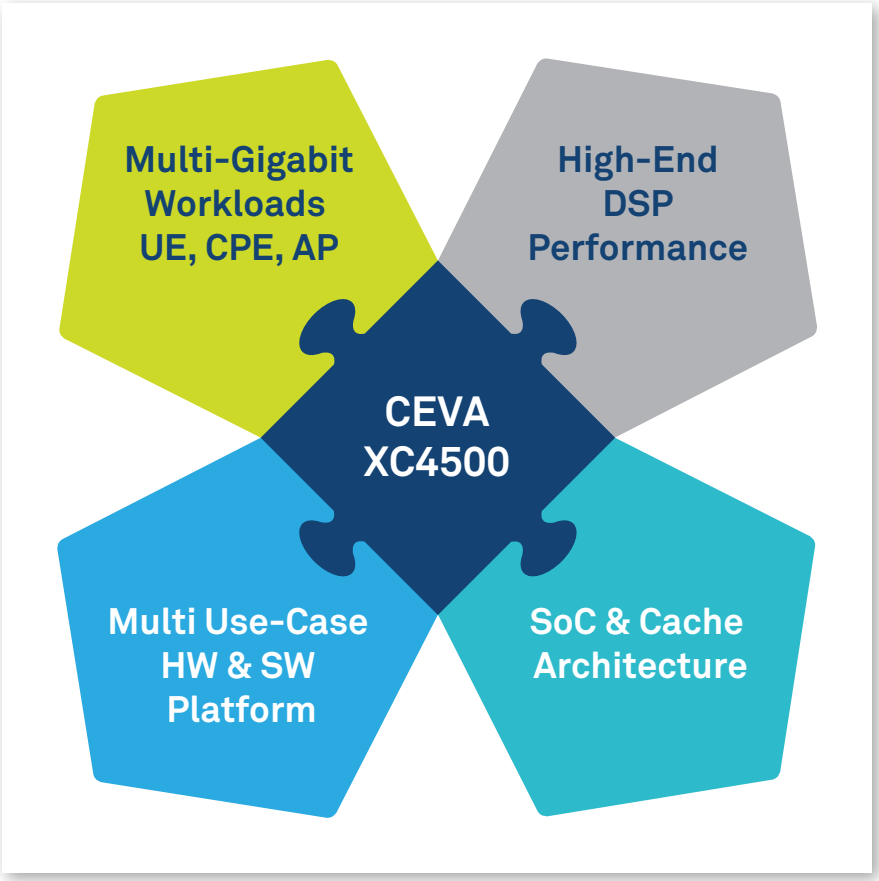
CEVA-XC4500 is the fourth generation vector processor IP from CEVA, designed to bring very low power, multi-gigabit, wireless modems capabilities to 5G-NR, LTE-A Pro and WiFi UE, CPE and Access Points.

Key Benefits

- **Meets the demanding requirements** of very low power multi-gigabit mobile modem use cases
- **Reduces Time To Market** with CEVA-XC4500 based platform that includes a rich set of HW accelerators combined with extensive optimized SW communication libraries for all celluar standards
- **Extendible and versatile architecture** addresses gigabit modems for 5G-NR eMBB, Fixed wireless access CPE, Cellular-V2X and 802.11p DSRC, Wi-Fi 11ax/ac 4x4 & 8x8 MS and AP, and Automotive Radar & Lidar

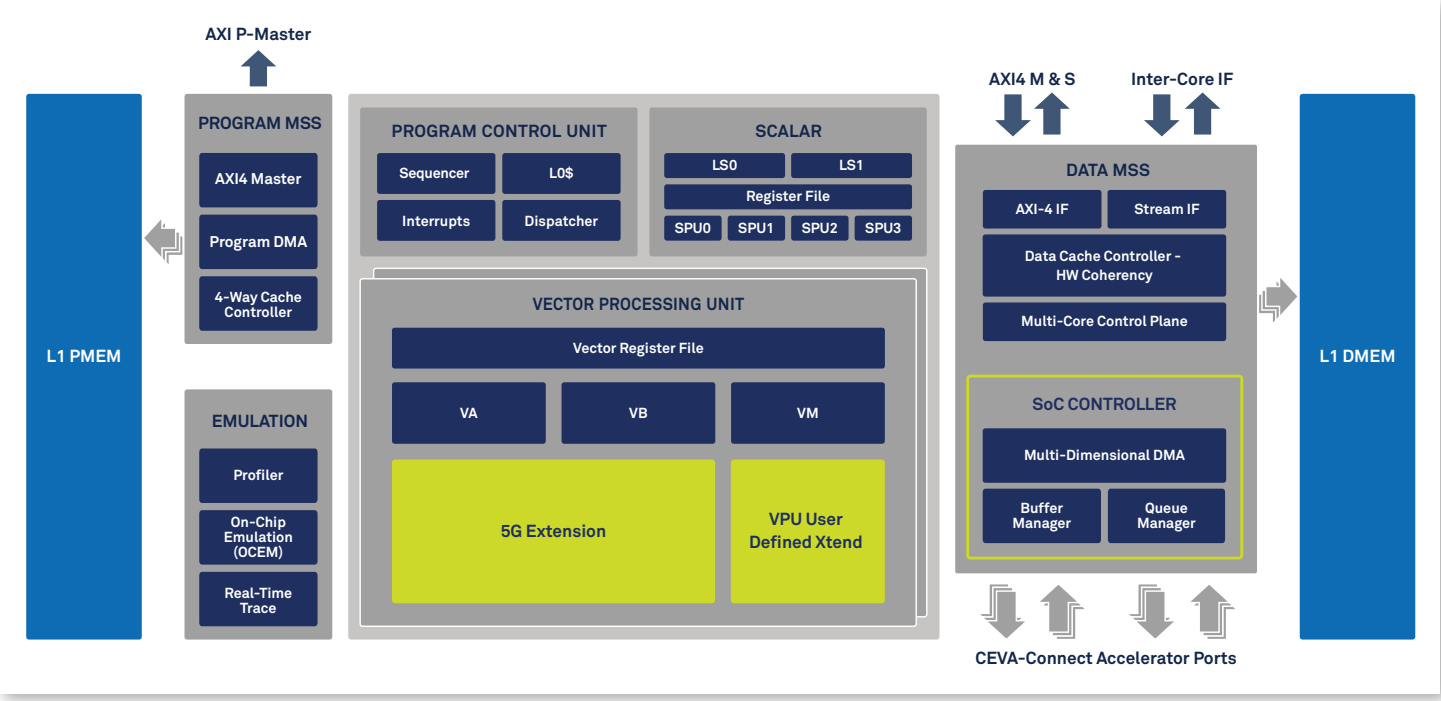
Applications and use-cases

- 5G-NR & LTE-A Pro UE
  - eMBB, URLLC
  - FWA (Fixed Wireless Access) CPE
  - C-V2X (Cellular V2X)
- Wi-Fi 802.11ax/ac/ad Access Point
- V2X DSRC 802.11p
- Satellite modems
- Wireline G.Fast, G.hn. xDSL



Cellular Modem HW accelerators available for CEVA-XC4500

Module	3G	LTE-A	LTE REL-12	3GPP-NR 5G
FFT /DFT		●	●	●
MLD MIMO Decoder		2x2, 4x4	2x2, 4x4	●
Vector Mac Unit			●	●
5G AI Processor				●
LLR Coprocessor		●	●	
Turbo-Decoder	●	●	●	
Viterbi Decoder	●	●	●	
5G LDPC Encoder/ Decoder				●
5G Polar Encoder/ Decoder				●
Fast Walsh –Hadamard Transform	●			
3G Despreader/ Descrambler	●			



CEVA-XC4500 5G architecture diagram

Architecture Highlights

Core features

- Runs at 1.2 GHz in 16nm.
- Fully programmable DSP architecture incorporating unique mix of VLIW and SIMD vector capabilities
- 13-stage pipeline enables very high speed for the most extreme use cases
- 8-way VLIW provides optimal hardware utilization
- Extremely powerful vector processor supports fixed- and floating-point operations with 64 MACs per cycle
- Rich Instruction set supports multiple precision integer, pseudo FP and IEEE FP real and complex operations to offer the most appropriate precision vs performance tradeoff for specific algorithms
- Dedicated instruction set (ISA) for 5G-NR eMBB UE and LTE-A Pro

System features

- AMBA 4 compliant matrix interconnect
- Comprehensive multicore support with ACE-compliant cache coherency
- Hardware/software partitioning delivers exceptional power efficiency while maintaining software flexibility with Queue and Buffer Managers and FIC interfaces
- Rich set of optimized SW Libraries and HW Accelerators for 5G-NR, LTE-A Pro, 3G, Wi-Fi 11ac/ax UE and AP

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