



Introducing CEVA-XC16

Non-NDA

www.ceva-dsp.com

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Corporate Introduction



Licensing IP since 1991
Powering ~1bn devices annually



NASDAQ:CEVA



Strong, profitable
~\$150m cash, no debt



>380 employees



R&D centers
Israel, France, U.S. & U.K.

Worldwide Operations



Global Reach Through Local Presence;
All direct CEVA employees

Our Technologies

Cellular

5G DSP-based platforms for smartphones, RAN and cellular IoT



IoT Connectivity

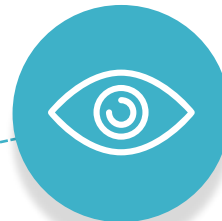
Comprehensive platforms for Bluetooth and Wi-Fi



Powered by
CEVA®

Camera sensors

DSPs for computer vision & imaging, AI processors & inferencing software (CDNN)



IMU sensors

Software & algorithms
Sensors fusion, management, activity detectors



Microphone sensors

Audio DSPs, voice algorithms, speech recognition, audio AI



Wireless Connectivity

Smart Sensing

>1 Billion CEVA-powered Devices Annually



U.S. Flagship
Smartphone

SAMSUNG

LG

mi

realme

Shark IQ ROBOT

LG

Virgin media



fitbit

Google

oppo

PHONAK

JBL

CREATIVE

mi

reolink

SAMSUNG

Introducing Gen4 CEVA-XC and CEVA-XC16



Introducing Gen4 CEVA-XC Architecture

The World's Most Powerful DSP Architecture

- ▶ Much more than a DSP core – a complete computing platform
- ▶ Innovative multithread and multicore architecture with dynamic vector computing resource allocation
- ▶ New and enhanced micro-architecture reaching 1.8 GHz @7nm
- ▶ Scalable to address a wide range of applications
 - ▶ 5G intelligent RAN, 5G endpoints, High-end Wi-Fi AP, Massive AI, Radar and Lidar

2.5X

Performance*

1.5X

Performance /
Area*

**Multi
thread**

1.8GHz

The CEVA-XC16 Multicore DSP

Cutting Edge 5G Processor for Advanced gNB Architecture



- ▶ First DSP processor based on Gen4 CEVA-XC Architecture
- ▶ Best in class DSP enabling and meeting the extreme performance requirements of next generation 5G NR architectures
- ▶ Designed leveraging our unique expertise in DSP and from close partnership with world-leading wireless vendors
- ▶ Scalable multicore / multithread architecture to address a wide range of applications
 - ▶ Cloud RAN, macro cells, DU acceleration, Open RAN, small cells, BBU pooling, massive MIMO RRUs, FWA, 802.11ax Wi-Fi AP

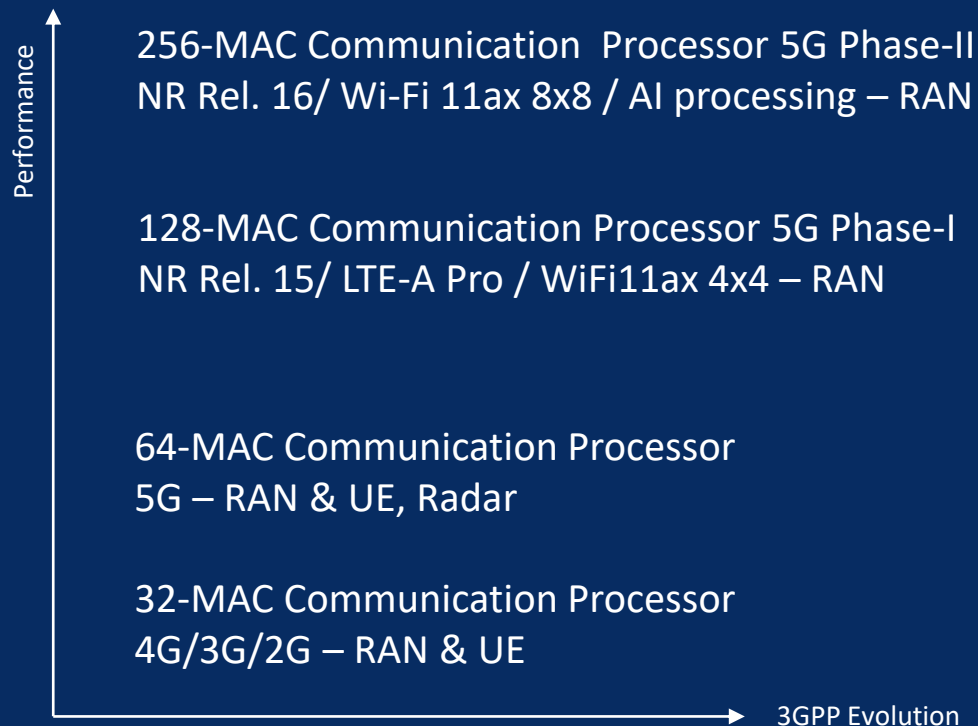
1,600
GOPS

256
MAC

1.8GHz

CEVA-XC Vector DSP Roadmap

A strong foundation for the RAN and UE markets



5G NR Phase II - The Need for Flexible and Powerful SDR Platform

The ever-increasing need for higher data rates and numerous operating modes calls for a scalable and flexible architecture that can support:

Massive Processing & Aggregation

1.

- ▶ Massive BBU aggregation and pooling
- ▶ Mix of carriers/bands of different width in both sub-6 and mmWave, multi-RAT supporting 5G NR & LTE
- ▶ Massive MIMO and advanced beamforming

Various Network Topologies

2.

- ▶ From D-RAN to C-RAN to V-RAN
- ▶ Emerging OpenRAN based architectures
- ▶ DU Acceleration
- ▶ Massive MIMO RRUs
- ▶ In-building, Small-cells, private networks and verticals

Multi User and Multi Computing Tasks

3.

- ▶ Multi User processing supporting fine user allocations & massive single user resources
- ▶ Fine slot allocations and short latencies for uRLLC and mission critical use cases
- ▶ Multi node support with network slicing supporting Industry 4.0 and eHealth applications

5G Standard and Network Evolution

4.

- ▶ 3GPP Release 15 now being deployed
- ▶ Phase II Release 16 and 17 expected this and next year
- ▶ Hardwired solution will not do. Need a robust SDR platform serving future RAN needs throughout the decade

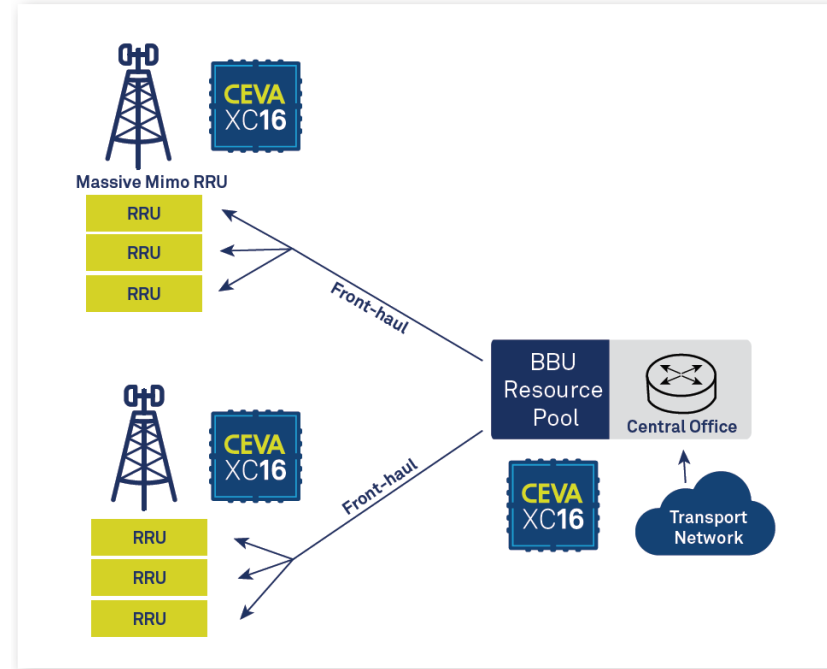
CEVA-XC16 Architecture



A New Architecture for the Debut of the 5G NR Decade



- ▶ CEVA-XC16 was designed specifically to address immense 5G NR baseband processing challenges
 - ▶ Design inputs from leading Tier 1 OEMs
- ▶ Looking forward for C-RAN/D-RAN deployments
- ▶ Targeted for both DU side for BBU pooling aggregation, or RRU side for large MIMO dimensions and carrier aggregation
- ▶ Combination of 256-MAC flexible vector unit and unprecedented DSP clock speeds makes it the #1 baseband crunching machine
- ▶ Dynamic support of mass multi-user and large single user allocations → multi core/thread



CEVA-XC16 - Multithreading for Multi Challenges

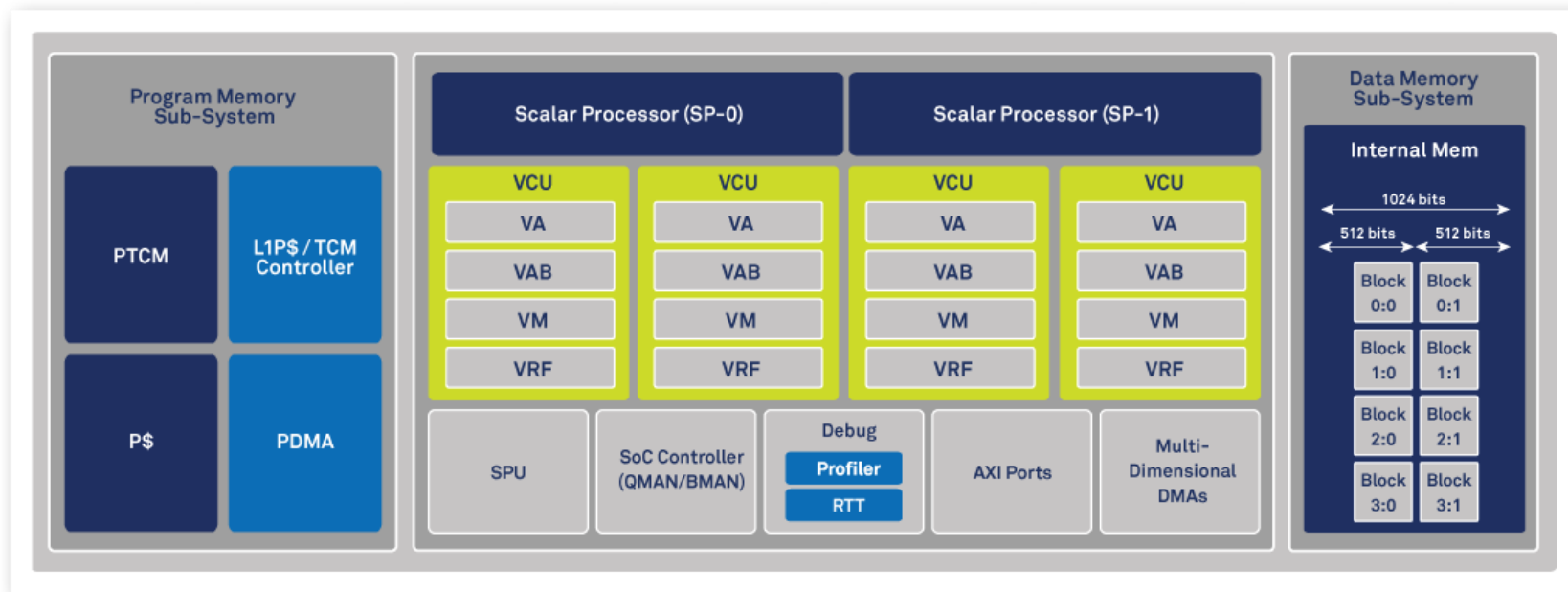
CEVA-XC16 Architecture Highlights



- ▶ Based on Gen4 CEVA-XC Architecture
- ▶ Increased length pipeline and physical design support to achieve 1.8GHz @ 7nm
- ▶ Quad vector processor units supporting up to 256 MACs per cycle
- ▶ Dual scalar processors for true multithreading
- ▶ Dynamic allocation of vector units to scalar processors:
 - ▶ QV mode: 4 vector units assigned to SP-0, SP-1 functions as scalar only
 - ▶ DV mode: 2 vector units assigned to each of SP-0, SP-1
- ▶ New optimized ISA for accelerating key functions
 - ▶ Dedicated FFT and symmetric FIR ISA
 - ▶ x2 improvement in Complex FIR and Matrix Multiplication (vs. XC12)
- ▶ 1.5 Performance/Area increase over CEVA-XC4500 and CEVA-XC12
 - ▶ Translates to 35% area savings for a large cluster of cores (typical for base-station silicon)



CEVA-XC16 Architecture Diagram

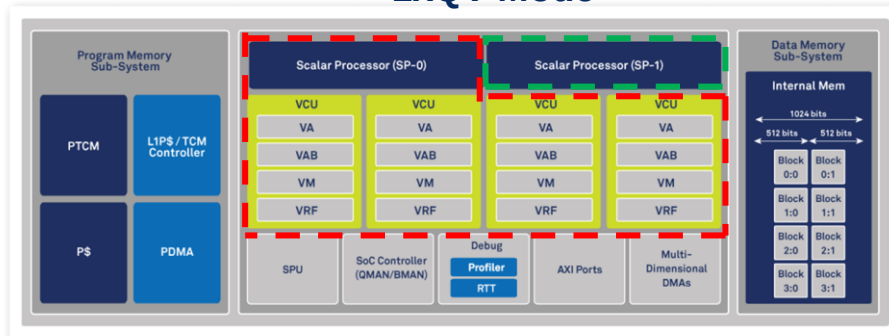


Dynamic Multicore

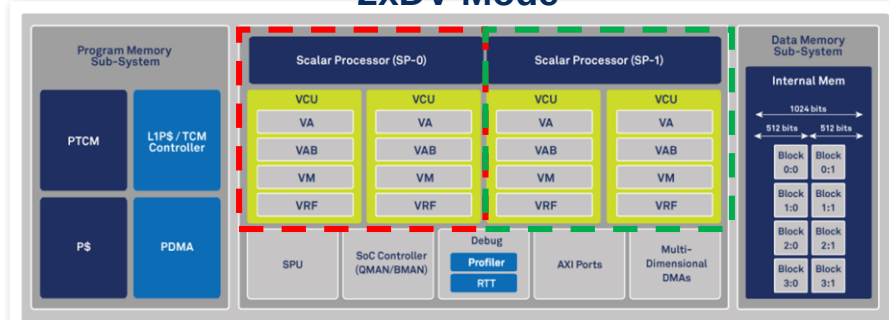


- ▶ Gen4 CEVA-XC Dynamic VCU allocation
- ▶ Highly efficient use of precious Vector Unit resources for enhanced MAC utilization
- ▶ Mode 1: 1xQV (Quad Vector)
 - ▷ All VCUs assigned to SP-0
 - ▷ SP-1 runs in parallel as controller
 - ▶ Can act as PHY controller and control external HW accelerators
- ▶ Mode 2: 2xDV (Dual Vector)
 - ▷ SP-0 and SP-1 are assigned two VCUs each
 - ▷ Symmetric processing flows
- ▶ Fast run time mode switching (few cycles)

1xQV Mode



2xDV Mode



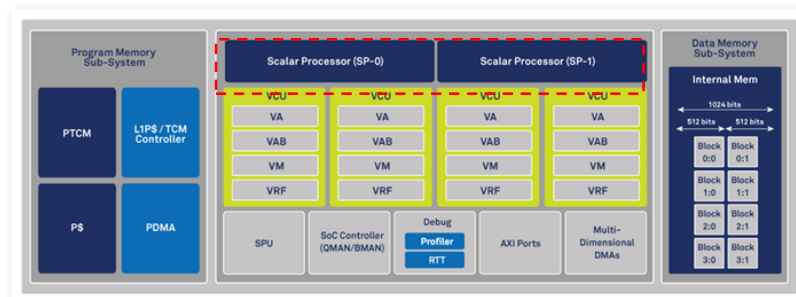
Multithreaded Scalar Control Architecture



- ▶ CEVA-XC16 integrates Dual CEVA-BX scalar processors, CEVA's latest generation common scalar architecture
- ▶ Compiler friendly architecture with a large common register file, full ISA predication and native support for all C types
- ▶ LLVM based compiler
- ▶ Second generation dynamic branch prediction (BTB)
 - ▷ Simple loop handling with zero-latency loops
 - ▷ Integrated loop buffer
- ▶ Code size reduction features
 - ▷ Fine tuned encoding scheme
 - ▷ Code Symbol Table
 - ▷ Partial loop execution

30%
Better Control
Performance*

30%
Code Size
Reduction*



SW Migration Path to CEVA-XC16



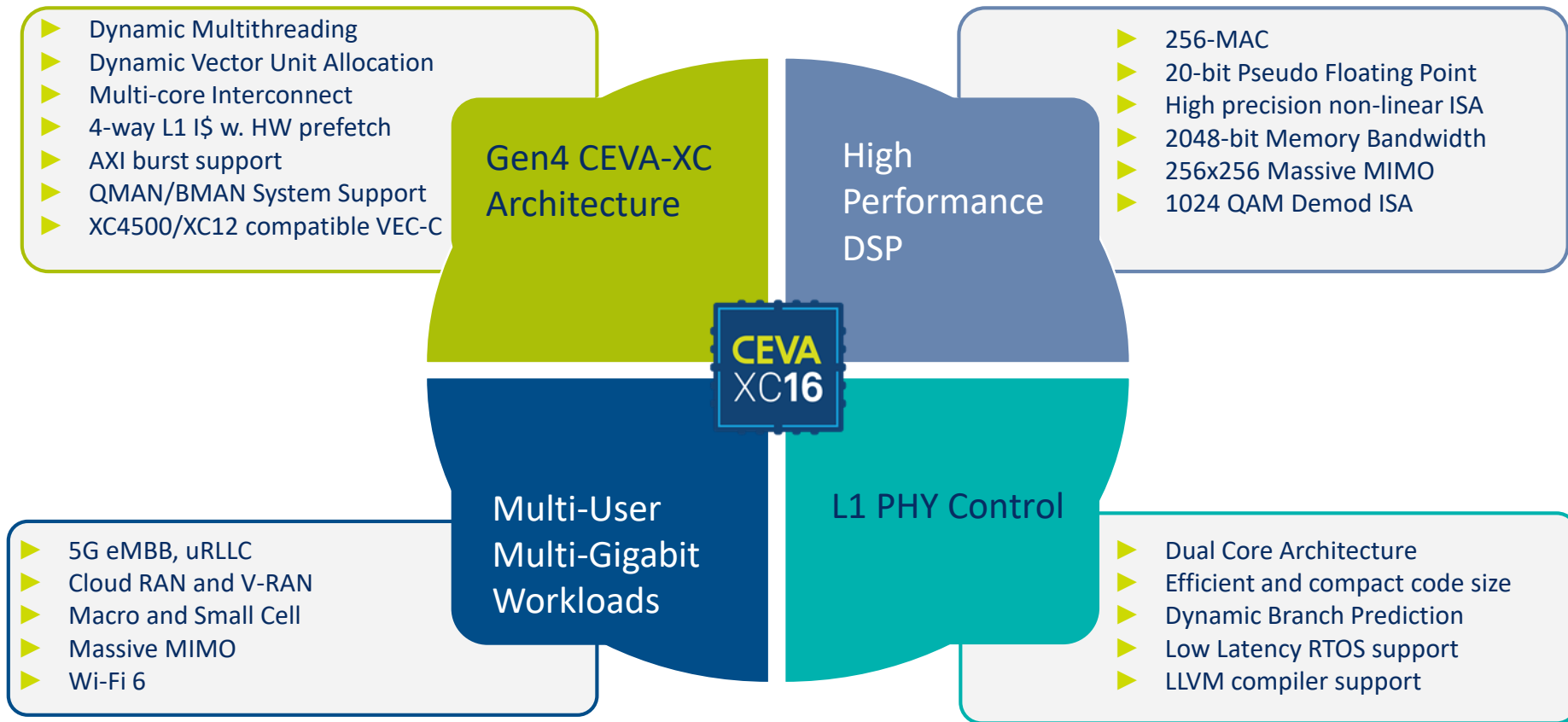
- ▶ CEVA-XC16 is VEC-C compatible with CEVA-XC4500 & CEVA-XC12
 - ▷ Legacy code can be compiled to and executed on XC16
- ▶ Each CEVA-XC16 can execute simultaneously two CEVA-XC4500 threads !
- ▶ Legacy one time code conversion
 - ▷ Following this one time conversion legacy code can be continuously maintained for XC4500, XC12 and XC16



Summary



CEVA-XC16: Putting It All Together



Thank You



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