



CEVA-XS Platform

Configurable, Low-Power, Highly-Integrated SoC Platforms

Target Markets

- › Cellular Communications
- › Mobile Multimedia Application Processing
- › Home Theatres and High Fidelity Audio Systems
- › VoIP Multi Channel Applications
- › Servo Controller for Storage Devices

Overview

The CEVA-XS™ platform is a low-power, highly-integrated SoC subsystem designed to reduce development costs and time-to-market for customers designing next-generation DSP-powered devices.

Built around the industry-leading CEVA-X DSP cores, the CEVA-XS platform uses industry standard system buses, offering designers the ability to add their own hardware blocks or connect the DSP to other systems present on chip.

CEVA-XS is a process and foundry-independent platform, with the ability to reuse and configure the technology for various market needs. It is a complete, verified hardware platforms that reduces development efforts, mitigates the risk of costly silicon re-spins and slashes time-to-market by twelve months or more.

CEVA-XS platform exploits multiple innovative power-saving techniques such as deactivating complete system modules and peripherals when not required, adjustable DSP system speed, decentralized inter-connect topology, level-two memory architecture and caching and selective hardware/software wake-up events.

With the addition of off-the-shelf software provided by CEVA and its CEVAnet 3rd Party technology partners, the CEVA-XS platform suits a wide range of applications such as Communications, Multimedia, VoIP, Storage and more.

CEVA-XS platform is available in two ultra-low power versions: CEVA-XS1100A, a low-cost platform optimized for general purpose DSP and communications applications and CEVA-XS1200A, combining all the features of the CEVA-XS1100A with additional features enhancing the system processing horse-power, such as a programmable 3D DMA co-processor and glue-less TDM interfaces.

CEVA-XS Platform Key Features

> Power Management

- System modules active only when needed
 - > Clocks are controlled and automatically stopped
- Reduced memory access
 - > Using two level memory architecture and caching
- Reduced load and traffic bus transactions
 - > Through decentralized interconnect topology
- Adjustable DSP system speed
 - > Software controlled DSP clock division / clock stop

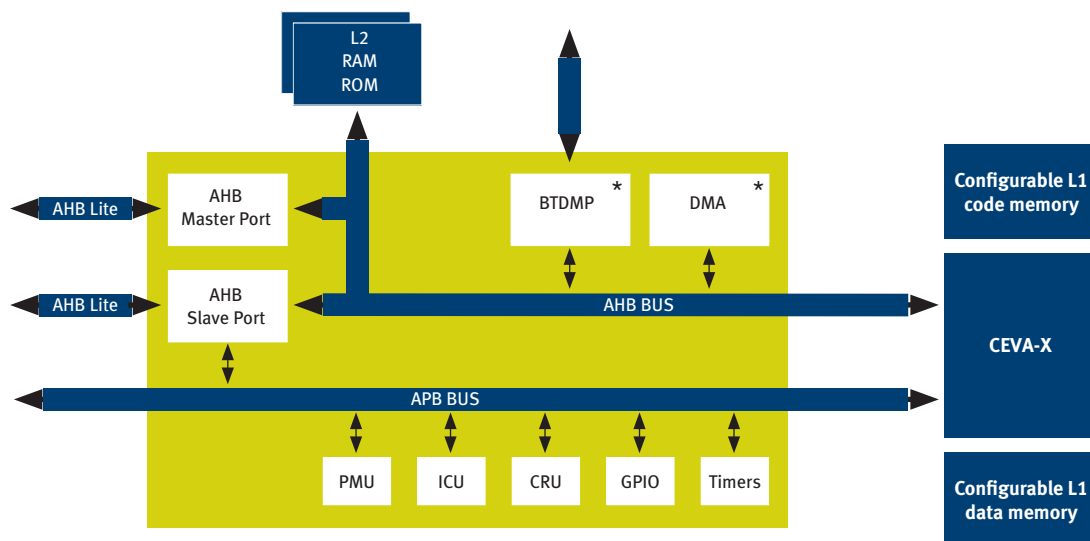
- > Software running at optimized clock frequency
- Standby to Active modes easily toggled
 - > Selective wake-up on various events, both hardware and software

> Easy SoC Integration

- Enables connectivity of external CPU systems to CEVA-XS environment
 - > Share peripherals on both CPU and DSP systems
 - > Share L2 memory between DSP and CPU
 - > DSP slave mode
- Glue-less interface to AHB bus protocols
 - > AHB-lite master port
 - > AHB-lite slave port
 - > APB bridge
- Easily extended with additional peripherals using external APB bridge

> Flexible Memory Architecture

- CEVA-XS provides two level memory architecture
 - > Level 1 – part of the CEVA-X DSP core memory subsystem
 - Program cache and data memory interface
 - > Interface to unified Level 2 memory
 - Two Level 2 memories can be accessed in parallel
 - Can be a combination of SRAM and ROM
- Sharing of memory between DSP and CPU saves resource
- Unified program and data with on the fly partitioning eases coding and reduces die size
- Eases application software development



* Only available on the CEVA-XS1200A

CEVA-XS Platform Block Diagram

› Rich Set Of Peripherals

- Comprehensive interrupt controller
 - › Masking, prioritization and sensitivity
 - › Interrupts can be generated by:
 - External sources
 - CEVA-XS peripherals
 - Software
- Timers & counters
 - › Configurable modes of operation including Watchdog
- Programmable General Purpose I/O (GPIO)
 - › 32 general purpose input/output pins
- Power management

Code Replacement Mechanism

- › Provides easy way to bypass application bugs without the need for silicon re-spin
- Eliminates recall of products through firmware upgrade
 - › On the fly software upgrades and updates

Enhanced Multimedia System Support (CEVA-XS1200A only)

- › Configurable and autonomous DMA engine for fast memory transfers significantly reduces power and increases overall performance
 - › Includes 3D data transfer capabilities with post modifications
 - › Programmable channels
 - › Event triggered DMA transactions
 - › Up to 64-bit data transfer
 - › Full access to all system components including:
 - L1 /L2 Memories, TDM ports and CPU peripherals
- Glue-less audio/voice streaming with Time Division Multiplex (TDM) ports
 - › Sophisticated, full-duplex, standard connectivity of multiple digitized data channels via single 4-6 wire interface
 - › Flexible implementation supporting most industrial standards of serial interfaces (e.g. PRI, E1, T1, IOM-2, I2S, AC97)
- Enabling differentiation using Co-Processor bridge (AHB slave)
 - › Extends DSP systems with user's own hardware blocks

CEVA-XS Platform and Tools Support

- › CEVA-XS Platform is fully supported by CEVA software and hardware tool suite, including a complete set of software development tools such as a C-compiler, full-feature debugger and 2 different simulators.

CEVA-XS Platform Highlights

- › Highly-integrated DSP-based SoC platform
- › Combines a CEVA-X DSP core with a rich set of peripherals, interconnections and interfaces
- › Glue-less AHB-compliant interfaces to CPU systems
- › Two interfaces to Level-2 memories, shared between DSP and possible CPU
- › Targets mobile applications using power reduction techniques and modes of operation
- › Complete set of DSP peripherals, including:
 - › Power Management Unit
 - › Interrupt Control Unit
 - › Timers
 - › Code Replacement Unit
 - › General Purpose I/Os
- › Programmable 3D DMA engine, built for multimedia applications, off-loading all data transfers from the DSP
- › Time Division Multiplex (TDM) ports for glue-less connectivity of any standard serial interface

The CEVA-XS hardware development tools include:

- CEVA-XS test chips, connected to the debugger via JTAG ports
- A complete application development board with complete Audio, Video and Imaging interfaces
- Connectivity to an ARM integrator board
- Connectivity to a FPGA chip and FPGA daughter card for application SoC verification



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