



# CEVA-SGMII Serial GMII Connectivity IP

## Features

- › 4 pin, 1.25Gbps Serial GMII interface, with optional transmit DDR clock
- › Fully compliant SGMII protocol layer
- › Ultra low power SerDes Core
- › 30mW on 0.13µ process
- › Low area SerDes core
  - 0.45 mm<sup>2</sup>, 0.13µ process
- › Robust Link Performance
  - Total transmit jitter less than 25%
  - CDR receiver tolerance greater than 65%
  - +/- 2000ppm drift tolerance
- › Designed for Test
  - At speed BIST in SerDes core
  - Full scan chain coverage for RTL

## Deliverables

- › GDSII for SerDes core, with simulation models and physical views including LEF, LIB
- › RTL package for SGMII PCS Layer, with physical design scripts
- › Available on TSMC 0.18µ & 0.13µ Generic CMOS processes

## Overview

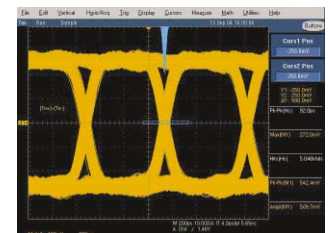
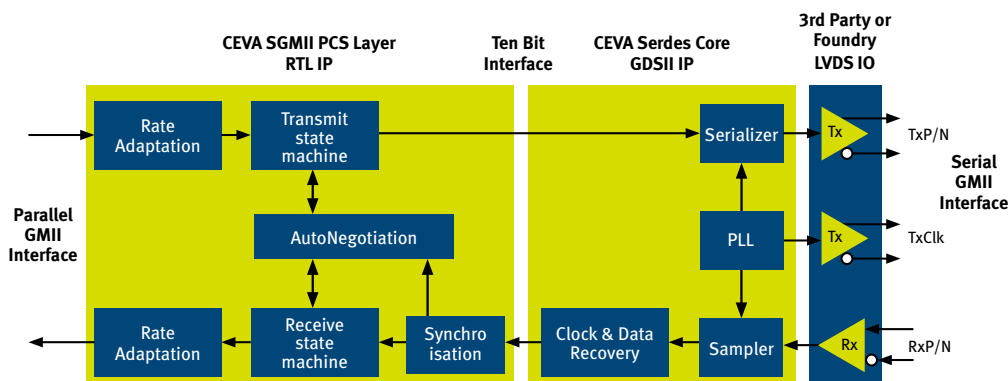
CEVA-SGMII Intellectual Property provides a low power and robust solution for connecting external Gigabit Ethernet PHY chips to the corresponding MAC layers embedded in a separate SoC, via the Serial GMII interface standard.

By combining the silicon-proven ultra low power CEVA Serialiser/Deserialiser (Serdes) technology with a fully compliant SGMII protocol layer, CEVA-SGMII IP is an ideal solution for applications looking to integrate SGMII ports without relying on a separate clock line to time the data transfer and hence delivers the lowest power and pin budget possible.

CEVA-SGMII is delivered in the form of a GDSII hard macro incorporating the PLL, serialiser, deserialiser and Clock & Data Recovery (CDR) circuitry, along with an RTL IP package for the SGMII PCS layer.

Initially targeted to both TSMC 0.18µ and 0.13µ Generic CMOS process, CEVA-SGMII is also portable to alternative processes.

Backed up by the experienced Wireline design team, CEVA's silicon-proven serdes technology substantially reduces the risk and time required to incorporate SGMII ports into ASICs and standard semiconductor products.



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