



**CEVA SAS 2.0  
Target Controller IP**

**Highlights**

- › SAS2.0 Target Controller IP
- › For SSD and other Target devices such as Tape/Optical Storage
- › Provide SSP and SMP functions
- › 6.0/3.0/1.5Gbps Rates supported
- › Comprehensive support for SCSI SBC-2 End-to-End Protection (DIF)
- › Robust Data Path Protection with overlapping CRC / Parity
- › High Performance, full duplex DMA, with IEEE 1212.1 Block Vector Structure Scatter/ Gather support
- › Comprehensive configuration, control and alarm / status monitoring, providing flexibility for Vendor Specific features
- › Flexible Phy Control Layer for integrating with industry leading 6Gbps serdes solutions, such as Snowbush serdes IP

**Introduction**

With ever-increasing requirements for higher performance and higher reliability, the enterprise storage industry is rapidly evolving from parallel SCSI to Serial Attached SCSI. Providing double the line rate of 6Gbps compared to the previous generation, SAS 2.0 has now become the preferred choice for new SAS products designs.

The CEVA-SAS 2.0 Controller IP provides both Target and Initiator functionality. Suitable for narrow or wide port implementations with 6.0/3.0/1.5Gbps data rates, it supports many enterprise level features including SCSI SBC-2 End-to-End Protection (DIF) and high performance, full duplex DMA with IEEE 1212.1 Scatter/Gather.

Reflecting the system complexities of SAS, it provides a comprehensive configuration, control and alarm / status monitoring interface with extensive metric counters and error injection facilities. With complete programmable control for Vendor Specific features, the CEVA-SAS 2.0 Controller IP enables customers to create highly differentiated and robust SAS 2.0 products

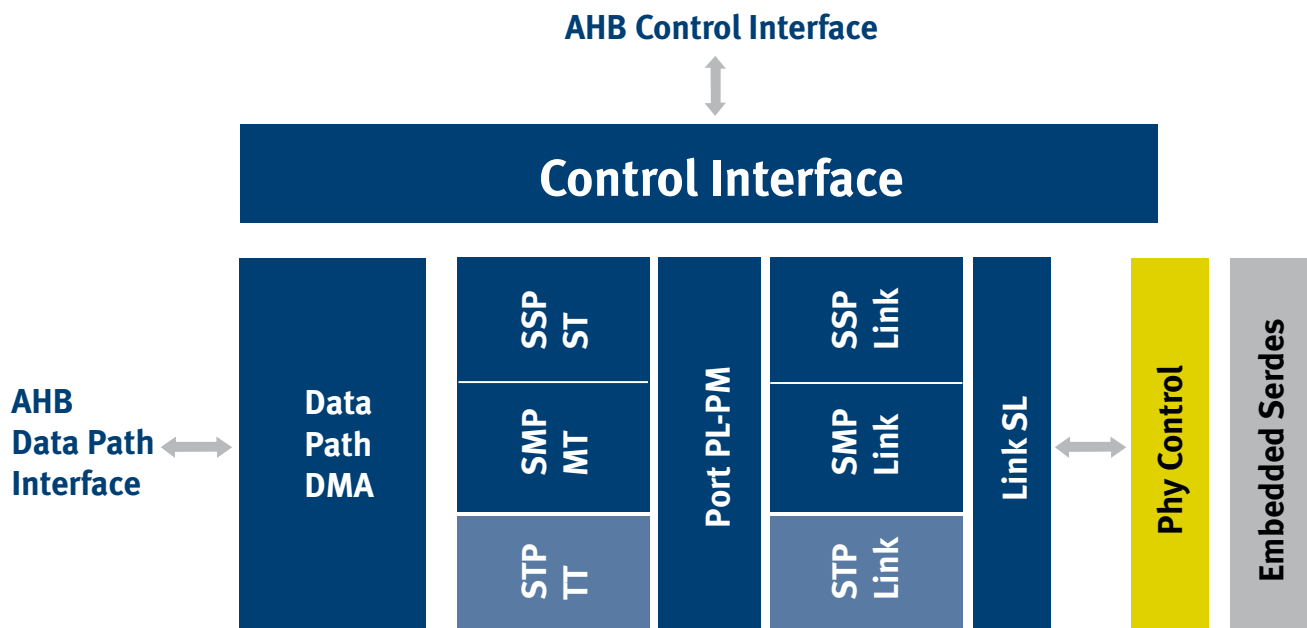
Supplied with a flexible Phy Control Layer, the CEVA-SAS Controller IP can be integrated with in-house serdes technology or leading 3rd party serdes technology, such as that provided by Snowbush or the embedded serdes functions inside the Virtex V/VI Xilinx FPGAs and Altera Stratix IV FPGAs.

The CEVA-SAS 2.0 Target Controller IP is primarily aimed at enterprise SSD Controller ASICs and FPGAs.

Accompanied by an FPGA Development platform which is driven by CEVA-SAS Tool software, the CEVA-SAS2.0 Target Controller IP is an ideal solution for customers looking to develop the next generation of Enterprise-SAS SSDs products.

### IP Deliverables

- › Verilog RTL package for CEVA-SAS2.0 hardware, including simulation environment, physical design scripts, datasheet
- › ANSI C package for CEVA-SAS Tool example software
- › Xilinx Virtex VI design materials, including programming file for ML605 FPGA board



CEVA-SAS 2.0 Block Diagram

## CEVA-SAS2.0 Target Controller IP Features

### › SASChannel Controller hardware IP encompassing SSP and SMP for Target

### › 1.5 / 3.0 / 6.0 Gbps Rates supported

### › Supports Standard and Non-standard IDENTIFY address Frames, BROADCAST Primitives and NOTIFY Primitives

### › OPEN Connection Management

- Hardware processing of OPEN address frame with automatic generation of OPEN\_ACCEPT or OPEN\_REJECT.
- Full software observability of OPEN address frame contents
- Full software control to set the FEATURE bits, the ARBITRATION WAIT TIME field and PATHWAY BLOCKED COUNT field
- Standard Open Timeout plus programmable timeout for connection requests that receive too many AIP primitives
- Automatic retry of OPEN address frames for OPEN\_REJECT (retry classes)
- Support decode of OPEN\_REJECT (ZONING VIOLATION)
- I\_T Nexus Loss timer
- Initiator Connection Response timer

### › CLOSE Connection Management

- Provides programmable Maximum Connection Timer and a Bus Inactivity Timer
- Intelligent issuing of DONE, based on Bus Inactivity Timer and whether there are frames to be transmitted and whether Direct Attach
- Programmability of the BREAK\_REPLY primitive capability

### › SCSI SBC-2 End-to-End Protection using DIF

- Flexible management of Reference Tag and Application Tag, including fixed Application Tag per Command, incrementing Application Tag per block within a Command and pass-through of pre-assigned Application Tag.
- Supports DIF Logical Block size up to 4Kbytes in increments of 512 bytes

### › SSP Support

- Full programmability of SSP frame Header
- Support all required SSP frame types: Command, Data, Transfer Ready, Response, Task
- Support for interleaved Short Response and Transfer Ready frames with Tx data frames
- Supports non-interlocked frame transmission for DATA frames
- Enables streaming of frames from sender by issuing 3 R\_RDY credits under normal conditions
- Complete Full Duplex operation, with independent transmit and receive DMA controllers
- Hardware checking of the source / destination hashed addresses in the SSP frame header.
- Hardware checking and insertion of offset in data frames
- Task frame fully programmable / observable
- Hardware checking of TPTT in Rx data frames
- Automatically generates RESPONSE frames on reception of data frames with incorrect TPTT field
- RESPONSE frame contents fully Software programmable

### › SMP Support

- Immediate transmission of pre-prepared SMP request frame immediately after receiving OPEN\_ACCEPT
- Immediate closing of the connection after receiving EOF
- Quick termination of potential 'hung' handshakes, using software programmable timer



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