

**CEVA SAS**  
Serial Attached SCSI IP

**Features**

- › SAS Port encompassing SSP/SMP/STP, in accordance with Serial Attached SCSI -1.1 (SAS-1.1), Rev 8, 2 Feb 2005
  - Provides all Protocol Layers, from Transport down to Link Layers
  - May be combined with CEVA PHY Layer or alternative PHY layer
- › 1.5 /3.0 /6.0 Gbps Rates supported
- › Suitable for Initiator or Target
- › Implemented as 4 Phy wide entity (Quad), which may be replicated for 8, 12, 16 Phy designs

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**Comprehensive SAS Solution**

CEVA SAS Intellectual Property provides a comprehensive solution to simplify the development of Serial Attached SCSI enabled SoCs. The combination of hardware and software IP plus expert advice significantly reduces the time to market and risk for new products entering this emerging market.

All three protocols defined by the SAS standard are supported, namely SSP (Serial SCSI Protocol), SMP (Serial Management Protocol) and STP (Serial ATA Tunnelled Protocol). All the layers within these protocols are provided, from Transport down to Link Layer. In addition, the PHY layer may be sourced from CEVA or 3rd party PHY technology may be incorporated via a gasket layer.

## Features (continued)

- › Programmable support for Narrow /Wide Port
  - Any permutation possible with Quad entity
- › High Performance, Scalable and Flexible Context Management
- › Supports Logical Block Size up to 4K in increments of 512 bytes.
- › Maximises System Performance through Enhanced OPEN / CLOSE Connection Management
  - Intelligent control over opening and closing of connections, retries and scheduling of frame transfers based on available commands and SAS fabric topology.
- › Minimizes loading on the IOP
  - Commands and Command Completions placed in circular Post/Reply queues, with Interrupt Coalescing
- › Robust Data Protection
  - SCSI SBC-2 End-to-End Protection using DIF
  - Data Path Protection using Byte-wide Parity
- › 32 bit AMBA for hardware interfaces
  - May also be customised or connected in using gaskets for alternative bus interfaces such as PowerPC CoreConnect.
- › Complete Software Stack with API
  - Interfaces to customer's Application Layer, abstracting the SAS environment below.
  - Implements SAS Discovery and Fabric initialisation functionality as well as the SCSI Initiator model.

## Deliverables

- › Verilog RTL package for SAS Channel & SASQuad hardware
- › C code package for SASQuad & PAL software

## Flexible & Scalable with High Performance

Due to the flexibility required to cope with the wide range of potential topologies within a SAS environment, some of the protocol functions are partitioned into software. This software is executed on a local embedded processor, which is shared over four SAS channels (i.e. a Quad channel arrangement). The CEVA-TeakLite core, with its low gate count, high code density, excellent bit manipulation features and split X/Y/Z memory space is ideal for servicing such a SASQuad arrangement and is incorporated as the default processor.

The I/O Context Management function is also shared over a Quad channel, with independent transmit and receive I/O Contexts to ensure high performance full duplex operation. A scalable design is provided which uses on-chip storage for a customisable number of I/O Contexts, augmented by expandable off-chip storage for larger systems. Hardware accelerated Context Lookup ensures maximum performance.

The architecture permits a highly flexible design for realising Narrow/Wide SAS Ports, spanning up to four channels in a Wide Port. Further, with this partitioning, software may be used to intelligently control the opening and closing of connections, retries and scheduling of frame transfers based on available commands and SAS fabric topology. The underlying algorithms maximise overall system performance.

The architecture supports more complex SAS topologies containing non-homogenous Targets, with parameters programmable on a per Target basis.

Adopting the popular AMBA interface, CEVA's SAS IP hardware interfaces may also be customised or connected in using gaskets for alternative bus interfaces such as PowerPC CoreConnect.

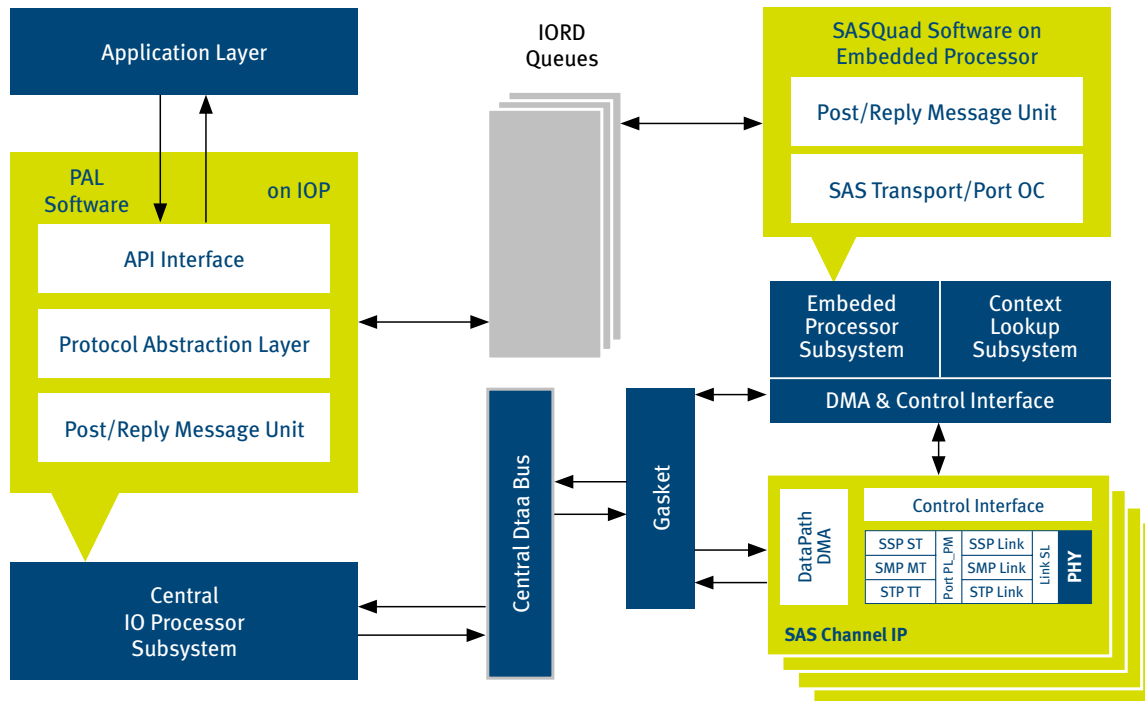
## Robust Data Protection

In addition to performance, robustness is ensured through SCSI SBC-2 End-to-End Protection using DIF, plus byte-based parity protection on the SAS data path. The architecture also supports advanced metric harvesting and debug features.

## Complete Software Stack with API

As illustrated in the diagram overleaf, the software accompanying the SAS hardware IP is split between the SASQuad software running on the local TeakLite and the Protocol Abstraction Layer (PAL) software, running on the main IO Processor (IOP).

## CEVA-SAS Block Diagram



CEVA's SASQuad software running on the CEVA-TeakLite embedded processor communicates with the Protocol Abstraction Layer (PAL) using Input Output Request Descriptors (IORDs). These Descriptors are communicated using Post-In, Reply-Out circular queues, with one queue spawned per SAS Port. The circular queue mechanism is used to its full extent to reduce overhead on the IOP, providing an interrupt coalescing scheme to optimise the communications. The circular queues reside in the main memory space of the IOP. When commands are thus transferred down to the CEVA-TeakLite embedded processor, further optimisation is performed to schedule the commands efficiently for maximum performance, effectively off-loading this processing from the IOP.

The PAL software provides a structured API interface for the Application Layer. It encapsulates SAS Discovery and Fabric initialisation functionality as well as the SCSI Initiator model. Hence, the customer is presented with a simplified abstracted interface to the SAS environment below. The PAL is written as common C code base and can be customized if necessary for specific customer features.



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