



CEVA LVDSn SERDES

LVDS Serdes Core IP

Key Features

- > Dual or Quad Serdes Core
 - LVDS2 – Dual Core, LVDS4 – Quad Core
 - 250Mbps to 1.25Gbps, depending on the instantiated PLL
 - With optional DDR serial clock output for SGMII type applications
- > Very Low Power
 - 30mW per Rx/Tx lane @ 1.25Gbps in 0.13μ TSMC-G process
 - 50mW per Rx/Tx lane @ 1.25Gbps in 0.18μ TSMC-G process
 - 30mW per Rx/Tx lane @ 622Mbps in 0.18μ TSMC-G process
- > Low Area
 - 0.6mm² per lane, 0.18μ process
 - 0.45mm² per lane, 0.13μ process
- > Robust Link Performance
 - Total Transmit Jitter < 25% UI
 - CDR receiver tolerance > 65%, K28.5 symbol
 - +/- 2500ppm drift tolerance

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Overview

CEVA LVDSn SERDES is the flexible, very low power serdes IP from Ceva. When combined with general purpose high speed LVDS buffers, this IP provides robust integrated serial links from 250Mbps to 1.25Gbps, depending on the instantiated PLL. With each serdes core incorporating up to four 10-bit parallel-to-serial and serial-to-parallel lanes, CEVA LVDSn SERDES provides a layout-friendly building block which can be instantiated multiple times to create the number of desired lanes, giving a scalable solution.

Excellent noise immunity is provided by the digital CDR scheme, which incorporates a simple equalization algorithm to reduce the worst effects of ISI. It also incorporates a bubble reject algorithm to discriminate between genuine data transitions and noise or erroneous samples, resulting in exceptional receiver tolerance. (65% eye-closure).

In addition to standard serdes functionality, CEVA LVDSn SERDES also provides a clock output on the serial interface at half the line rate (i.e. DDR style). This is particularly useful for SGMII-type applications where some legacy devices may not be capable of extracting the embedded clock from the data stream. For high port density applications that do not require this output clock, a ‘slim’ version of the IP is available without this clock.

Designed with a digital centric architecture for low power and ease of integration on generic CMOS processes, CEVA LVDSn SERDES provides a low risk option for integrating serial links in ASICs and standard semiconductor products.

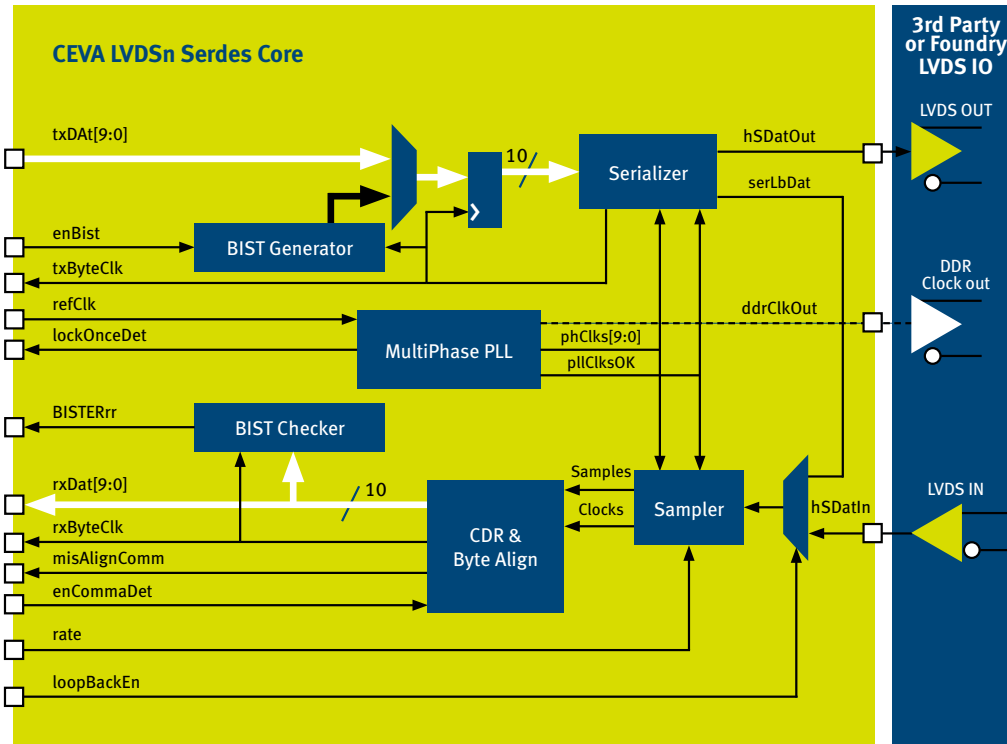
Key Features (continued)

- › Low Latency & Fast Lock
 - 38.5 to 41.5 UI Rx latency, Serial input to aligned symbol output
 - Less than 12 UI Tx latency, Parallel symbol input to serial bit output
 - Sub-200 UI lock time
- › Serial I/O
 - Single-ended CMOS core to IO interface
 - Designed to integrate with 3rd Party LVDS or LVPECL IO
- › Test features:
 - Serial loopback support
 - At speed BIST
- › Delivered Package:
 - GDSII macro for physical design, with physical views including LEF, LIB.
 - Available for TSMC 0.18µ-G and 0.13µ-G processes

Applications Include:

- SGMII PMA – may be combined with CEVA SGMII Protocol to give full solution.
- 1000Base-X Gigabit Ethernet PMA
- SONET/SDH (OC12/STM4) inter-chip and backplane links which do not require jitter transfer compliance (i.e. non re-clocking)
- xDSL & EFM based DSLAMs for Core to Line card backplane connections & Extension shelf connections
- Third Generation (3G) Base-Station line card backplane connections
- General chip-to-chip and backplane links

The following block diagram illustrates single channel operation only, for clarity. In practice, the Multiphase PLL circuitry is shared across the ‘n’ channels (e.g. n = 2 or 4) within the serdes core, with the other circuitry being unique to each channel.



CEVA LVDSn SERDES Block Diagram

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