



> CEVA-XC

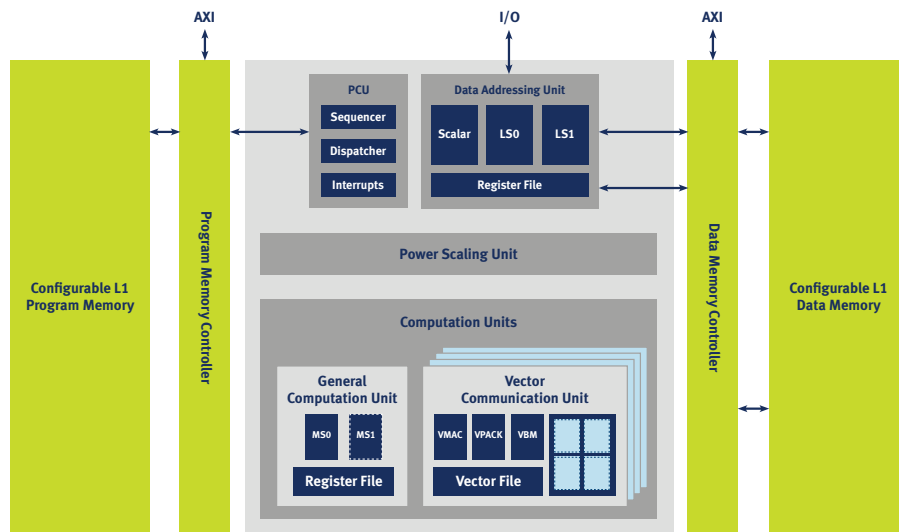
CEVA-XC Target Markets

- > Advanced 3.5 / 4G mobile modems:
 - Supports most demanding 4G standards: LTE class 5 and WiMAX II (IEEE 802.16m)
 - Various other wireless standards supported by SW: Wi-Fi, HSPA+, WCDMA, EVDO, GSM/GPRS, DVB-H, GPS
 - Target products: mobile handsets, Smartphones, MIDs, data cards
- > Wireless infrastructure:
 - Multiple LTE/WiMAX channels supported in a single core
 - Target products: Femtocells, Picocells, base-stations (BTS) and gateways

CEVA's Licensable DSP Cores

CEVA, Inc. is a leading licensor of programmable Digital Signal Processors (DSP) Cores and integrated-applications to the semiconductor and electronics industry. CEVA's product line includes a variety of DSP cores. Each core delivers a different balance of performance, power dissipation and cost, allowing licensees to select the ideal core in accordance with the targeted application requirements.

CEVA-XC™ is the sixth generation of licensable DSP Cores in the company's portfolio of leading edge technology. CEVA-XC builds upon the architecture of the CEVA-X™ DSP and is highly optimized for wireless applications. CEVA's DSP cores are long established in the market, having shipped in more than 1 billion devices to-date, including mobile handsets, Smartphones, portable media players, game consoles, netbooks, notebooks, home entertainment devices and others.



CEVA-XC Block Diagram

CEVA-XC - Industry's Highest Performance Communications Processor

CEVA-XC™ is a high-performance, low-power DSP processor designed and optimized for advanced wireless communications. This fully programmable architecture supports full transceiver processing for multiple air interfaces in software. A single CEVA-XC is capable of handling complete transceiver paths of LTE class 5 and WiMAX II (IEEE 802.16m), alongside 3G, 3.5G, Wi-Fi, GPS and MobileTV.

CEVA-XC is specifically designed to address the stringent power consumption, time-to-market and cost constraints associated with developing a high performance, next generation wireless communications processor. Utilizing an innovative scalable and modular architecture, CEVA-XC addresses the precise requirements of any 4G processor design, from handset terminals and mobile broadband modules through to wireless infrastructure equipment.

CEVA-XC eliminates the need for heterogenic architectures composed of multiple wireless coprocessors or accelerators which increase cost, time-to-market and software design complexity in wireless SoCs. In addition, CEVA-XC is coupled with a complete Integrated Development Environment including an optimizing C compiler, emulators, ESL tools and comprehensive software libraries to further reduce the associated integration effort and costs.

CEVA-XC Architecture Highlights

- Fully programmable DSP incorporating two computation units:
 - Vector Communication Unit(s)
 - › SIMD engine using 3-way VLIW
 - › Operates on 256-bit vector registers
 - › Up to four vector units are supported for a single CEVA-XC core
 - General Computation Unit
 - › Efficient DSP support for scalar data
 - › Efficient support for control and ANSI-C operations
- Extremely powerful computation capabilities
 - Up to 64 16x16-bit MAC operations, 128 16x8-bit MAC operations
 - Up to 64 arithmetic and logic operations per cycle
 - Up to 400 16-bit operations in a cycle
- Uniquely designed for wireless baseband
 - High flexibility SIMD programming model with intra-vector permutation capabilities
 - Optimized instruction set for wireless modems, including: matrix processing, MIMO detectors, filtering, complex data permutations and bit stream processing
- Efficient flow of the entire baseband application
 - Communication operations - Vector communication units deal with vectorizable data
 - General DSP operations - Complete support for general ANSI-C DSP functions, voice, audio, adaptive parameters, etc'

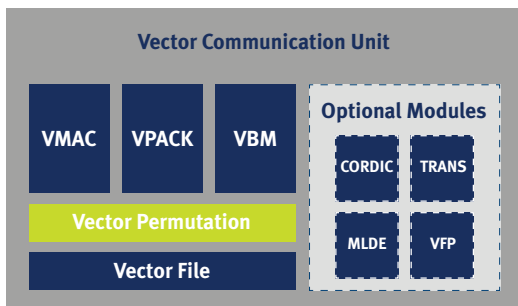
- Control code - Fully interruptible, conditional ISA, branch prediction, delay slots, etc.
- Memory accesses - Dual flexible LD/ST units with dedicated scalar unit

- › Scalable and configurable architecture
 - Scalable computation capabilities and memories
 - Configurable utilization of optional instruction sets
- › Complete memory subsystem
 - Includes tightly coupled memories (TCM), caches, AXI system interfaces, APB3 interface, 2D DMA, ECC support for L1 memories, emulation and profiling modules.
 - Ensures easy integration and optimal performance in Target SoCs

CEVA-XC Vector Communication Unit

CEVA-XC builds upon the architecture of the CEVA-X™ DSP by incorporating up to four modular Vector Communication Units, each:

- › Supports up to 3 parallel instructions
 - Each instruction operates on 256-bit registers
- › High flexibility in operations and data
 - Unique method for flexible SIMD operations
 - Vector permutation module
- › Optional instruction sets
 - Transmitter, floating-point, CORDIC and more
- › Advanced complex math capabilities
 - MIMO detectors, channel estimation, etc.
- › Dedicated support for bit-chain processing
 - Inter-leavers, scrambler, FEC encoders, etc.



CEVA-XC– Key Benefits

- › Leverages more than 20 years of experience in high-performance programmable DSP cores:
 - CEVA-X DSP at the heart of the CEVA-XC architecture is one of the industry’s leading DSPs deployed in WCDMA, TD-SCDMA, HSPA and WiMAX chips
 - CEVA’s DSP cores are shipping with four of the world’s top five handset manufacturers; Nokia, Samsung, LG Electronics and Sony Ericsson
- › Fully programmable processor optimized for wireless applications:
 - Supports LTE class 5 and WiMAX II complete transceiver paths on a single core in software
 - Single core solution for multiple wireless standards including: LTE, WiMAX, HSPA, WiFi, as well as existing 2G and 3G standards
 - Eliminates the need for multiple distributed engines and associated memories, buffers and on-chip data traffic
 - Low development effort using complete development tools chain
- › Ultra low power design optimized for mobile devices
 - Up to four times more power efficient than general purpose DSPs
 - System level Power Scaling Unit enables speed and voltage scaling at high level of granularity, including processing units, memory subsystem, debug and emulation units, TCM and caches
 - Supports multiple power-down modes, minimizing both dynamic and static power consumption
- › Scalable and configurable architecture
 - Targets both terminal and infrastructure applications
 - Allows licensees multiple alternatives and configuration options
 - Optimal balance between performance and cost

Software Development Tools

The CEVA-XC is accompanied by the advanced Integrated Development Environment (IDE) based Software Development Tools for embedded applications, supporting Windows, Linux and Solaris operating systems.

The Software Development Tools were developed in-house in parallel with the architecture definition to ensure compiler friendliness

Key features:

- Fully integrated IDE environment
 - Complete tools connectivity and setting
 - Fully featured editor
 - C level Browsing information
- Highly optimizing C Compiler
 - High-end optimization exploiting the core architecture for efficient code generation
 - DSP extensions and assembly intrinsics support for full control of the processor capabilities
- Advance Graphic User Interface Debugger
 - Cycle Accurate and Instruction Set Simulation of the core and memory sub system
 - Integrated graphic application profiler enabling optimal core and memories performance in C level
 - Emulation support with comprehensive debug capabilities (same look & feel as simulation)
- Optimized communication and DSP libraries
 - Ensures optimal performance and fast development cycle

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