



**CEVA-X ARCHITECTURE  
CEVA-X1641**

**CEVA-X1641 Target Markets**

- › 4G, LTE and WiMAX wireless baseband
- › Software Defined Radio, Multi-Mode Baseband
- › SmartPhones / PDAs
- › Video & Audio processing for mobile devices
- › VoIP Gateways & broadband modems
- › Home entertainment (Digital TV, HDTV, PVR, DVD)

CEVA-X1641 is a member of the CEVA-X DSP Cores family.

**CEVA's Licensable DSP Cores**

CEVA, Inc. is the world leading licensor of programmable Digital Signal Processors (DSP) Cores and integrated-applications to the semiconductor and electronics industry. CEVA's product line offers a variety of DSP cores. Each core delivers a different balance of performance, power dissipation and cost, allowing the customer to select a core preference in accordance with the targeted application requirements.

CEVA-X™ is the fifth generation of licensable DSP Cores in the company's portfolio of leading edge of DSP core technology solutions. It continues the line of the CEVA-Teak™, CEVA-TeakLite™, CEVA-Oak™ and CEVA-Pine™ DSP Cores.

## CEVA-X DSP – Key Benefits

### › High Performance at Low Power Consumption

The CEVA-X architecture has a unique mix of Very Long Instruction Word (VLIW) and Single Instruction Multiple Data (SIMD) architectures. The VLIW architecture allows a high level of concurrent instructions processing thus providing extended parallelism, as well as low power consumption. SIMD architecture allows single instructions to operate on multiple data elements resulting in code size reduction and increased performance. Low power consumption is also achieved in the CEVA-X by its instructions and dedicated mechanisms such as dynamic and selective units shutdowns and clock slow downs.

### › Scalability

CEVA-X is a scalable architecture from which multiple DSP designs are derived. Each DSP design is aimed to serve market-specific needs that are characterized by performance, power consumption and cost. Its architecture offers a long-term performance roadmap that allows re-usability of legacy software and hardware platform designs.

### › High-level Programming

CEVA-X architecture enables efficient programming in high level C-language that significantly reduces development cost and time-to-market. The CEVA-X architecture was designed in conjunction with the CEVA-X compiler tool. A most efficient and optimized C compiler is provided.

### › Soft Core

CEVA-X design implementations are Soft Core based, allowing the customer to select the optimal operating point in terms of die size, power consumption and performance. In addition, the customer has complete flexibility in selecting the foundry, process (e.g. 90nm, 65nm, 45nm) and complementary IPs.

CEVA-X IP incorporates fully automated design flow supporting mainstream EDA tools, significantly shortens time-to-market. CEVA-X design can be ported to an FPGA that can be used for product prototype, system integration, design acceleration and clarification

### › Development Tools, Software & Platforms

CEVA-X is supported by a complete set of software and hardware development tools. The software tools chain includes C Compiler, Assembler, Linker, Debugger, Simulator, Profiler, Utilities and DSP libraries; all under Integrated Development Environment (IDE). The hardware tools include various modular development system boards with associated accessories. A DSP hardware platform including the CEVA-X, DMA controller, CPU interfaces and a large offering of peripherals and interfaces is offered. Software and algorithms are provided by CEVA through its 3rd parties' network.

## CEVA-X1641 Advantages

### › High frequency –

over 700 MHz @ 65nm worst case conditions

(Note: Frequency depends on configuration, synthesis, foundry, process, operating conditions, and libraries)

### › Class-leading performance

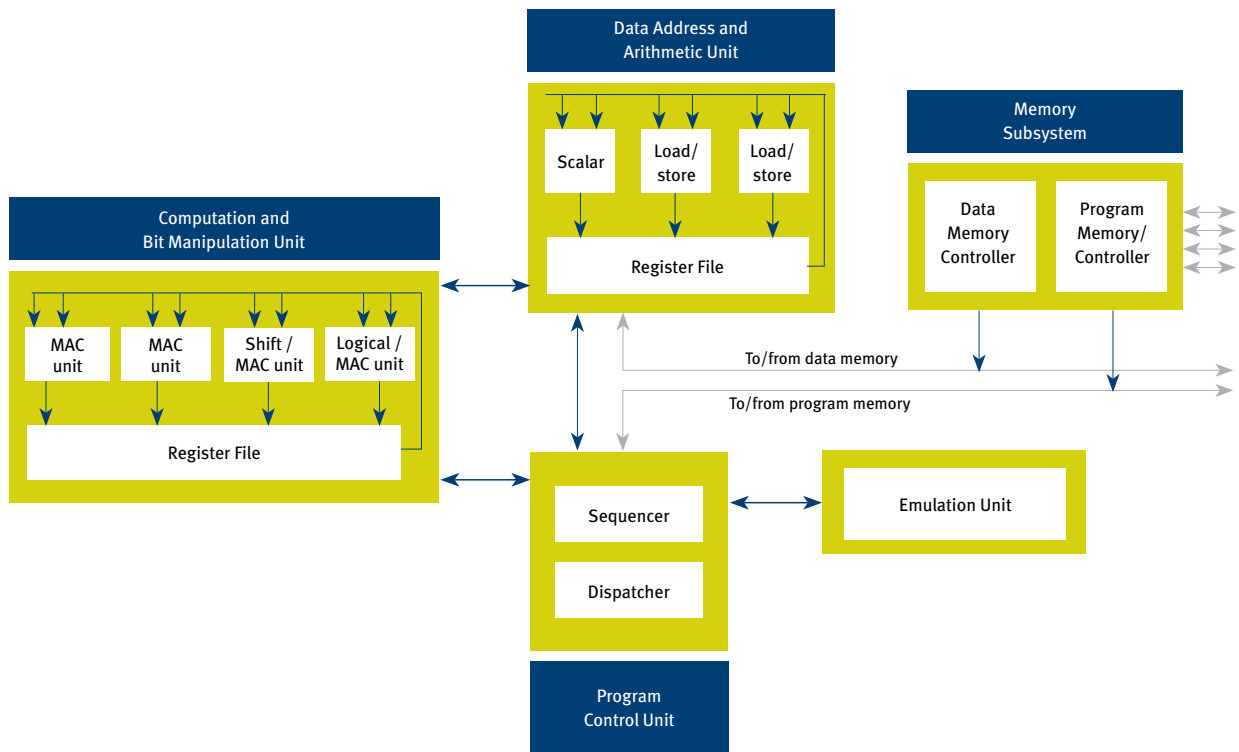
- Best Quad-MAC architecture
- Low power consumption achieved by the Core's instructions and a built-in mechanism, which shuts off any unused logic

### › Low power consumption achieved by the Core's instructions and a built-in mechanism, which shuts off any unused logic

### › Complete set of audio and voice codecs available through CEVA and its partners

### › Highly efficient C Compiler

### › Complete sets of software and hardware development tools

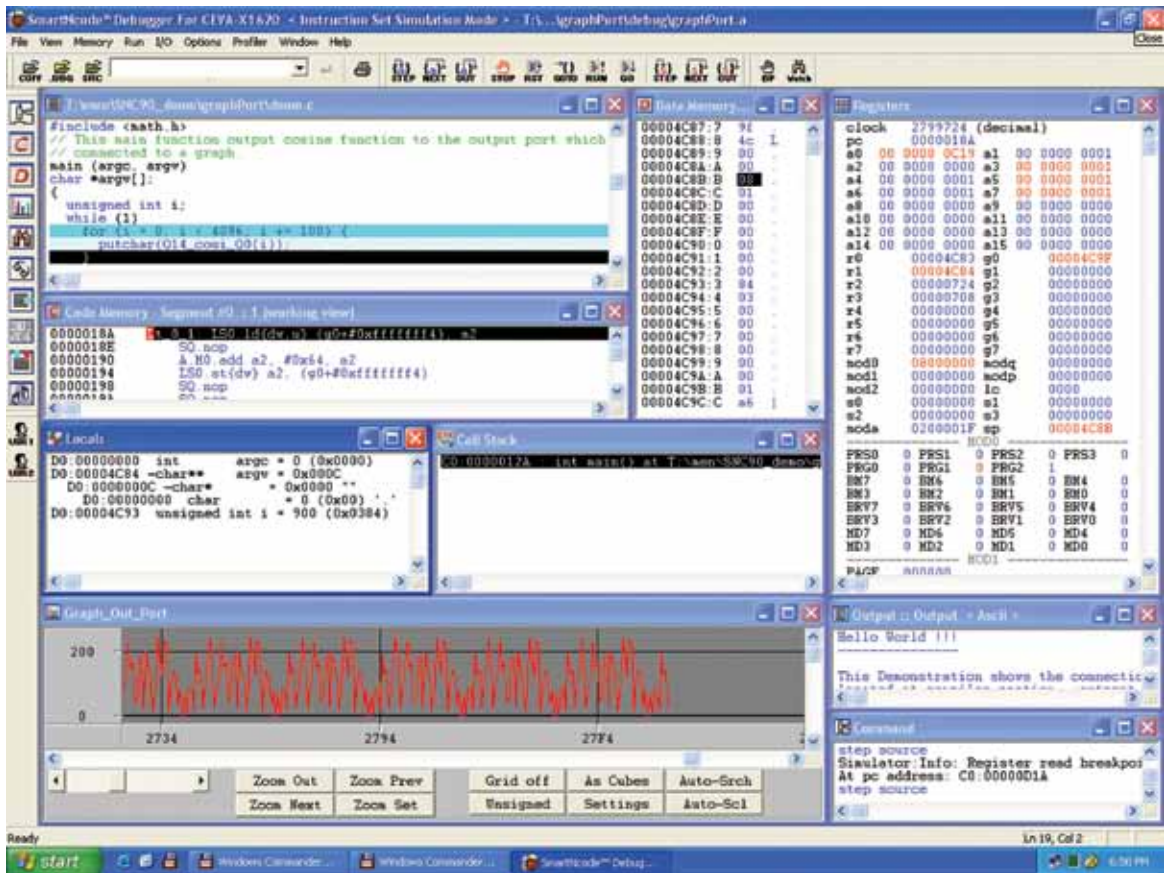


**CEVA-X1641 Block Diagram**

## CEVA-X1641 Architecture Highlights

- › Very Long Instruction Word (VLIW) and Single Instruction Multiple Data (SIMD) for enhancing DSP performance
- › Load/store architecture
- › Variable instruction width (16 or 32-bit) and variable length of instruction packets
- › Concurrent execution of up to 8 instructions in parallel
- › All instructions can be predicated
  - Conditional execution
  - Reducing cycle count and code size on control and overhead code
- › Computation unit contains
  - Four 16x16 bit two's complement MAC units, into 40-bit accumulators
    - Eight 8x8 multiplications in single cycle
    - Four 16x16 multiplications in single cycle
    - Double precision multiplications support
    - Data scaling after multiplications or prior to storing to data memory
    - Unique MAC unit connectivity allowing fast and accurate filtering
  - Four 40-bit arithmetic units
  - 40-bit logical unit
  - 40-bit Bit Manipulation Unit, including full Barrel Shifter and Exponent unit
  - Two 40-bit data pack and unpack units
  - Twenty Four 40-bit accumulators
  - Single cycle exponent evaluation of 40-bit values
  - Broad range of data byte operations
  - 1.2 cycle FFT butterfly
  - Single cycle Viterbi Add-compare-select
- › Data Address Arithmetic Unit
  - Two Load-Store units providing up to 64-bit data bandwidth to the data memories
  - Eight 32-bit data memory pointers
  - 32-bit scalar unit for integer operations and fast arithmetic calculations on Address registers
  - Variety of data addressing modes (Indirect, Bit-reversed, Direct, Indexed, Stack)
  - Enables linear and cyclic/modulo registers post-modification
- › Two Levels Memory
  - Up-to 4G-bytes address space
  - 64/96/160/288 K-byte level 1 program TCM and cache
  - 64/128K-byte level 1 data TCM
- › Byte addressable data space
- › Nine stages pipeline
- › Interfaces
  - Separate I/O space for peripherals
  - AHB-Lite interfaces (Data, Program, External transfer request) for easy integration in a SoC
- › On-Chip Emulation Module (OCEM) Memory Sub-system
  - Memory access arbitration
  - Controls AHB interface
  - Data DMA
  - Program DMA
  - Program cache controller

\* The BDTI<sub>sim</sub>Mark2000 provides a summary measure of DSP speed. For more info and scores, see [www.BDTI.com](http://www.BDTI.com). Score © 2008 BDTI.



Debugger Screen View

## Software Development Tools

The CEVA-X1641 is accompanied by the advanced Integrated Development Environment (IDE) based Software Development Tools for embedded applications, supporting Windows and Solaris operating systems

- › IDE Features
  - Project management
  - Makefile generation
  - Tools/project settings
  - Complete tools connectivity
  - Source control connectivity
  - Fully featured editor
  - Browsing information
  - Online help
- › Highly optimizing C Compiler
  - High-end optimization exploiting the Core's architecture for efficient code generation
- › Macro Assembler and Linker
  - Architectural restrictions checking and errors overcoming mechanism
  - Advanced mapping mechanism (Auto, Semi-auto and Manual)
  - Section overlay and multi-paging support
- › Advance Graphic User Interface Debugger
  - Instruction set and cycle accurate simulators
  - Emulation support (simulator's look & feel)
  - Source level debugging support – C and assembly files
  - User customizable DLLs for Debugger adaptation (Simulator extension, HW interface, etc.)
  - Parallel port, USB and JTAG emulation interfaces
  - Run-time violation detection by the simulator
  - Extensive breakpoint support, interrupt simulation and I/O support
  - Tight MATLAB Bi-Directional connectivity
  - Integrated graphic application Profiler
- › Various Utilities and Converters
  - Libraries generation
  - Produce various memory burnable formats

## Hardware Development Tools

### Evaluation and Development Platform

The Evaluation and Development Platform (EDP) is used for CEVA-X1641 based application development.

The EDP interfaces to a host PC through the JTAG interface (JBox) for full application control and contains the following:

- › On-board fast SRAM
- › On board 266MHz DDR SDRAM (without DIMM)
- › On board Flash memory
- › TFT LCD
- › EDP interfaces
  - UART
  - USB2.0
  - Parallel port
  - 6 channels audio out
  - Stereo audio in
  - Passive microphone
  - MMC/SD flash socket
  - CMOS sensor
  - Analog video in/out
  - Digital Video in/out
  - ARM core module connector (expansion slots)

### DSP on FPGA

A dedicated tool allows FPGA implementation of the CEVA-X DSP. The user can build an FPGA emulation model of the SoC containing the CEVA-X and other components, in order to verify the design before taping-out the actual silicon.



 [www.ceva-dsp.com](http://www.ceva-dsp.com)



---

#### PRINCIPAL OFFICES

##### USA

2033 Gateway Place, Suite 150, San Jose, CA 95110-1002,  
Tel: +1 (408) 514 2900 Fax: +1 (408) 514 2995

##### Israel

2 Maskit Street, POBox 2068, Herzelia, 46120, Israel  
Tel: +972 9 961 3700 Fax: +972 9 961 3800

##### Ireland

2nd Floor, 8-11 Lower Baggot Street, Dublin 2, Ireland  
Tel: +353 1 237 3900 Fax: +353 1 237 3923

© 2008 CEVA, Inc. All Rights Reserved. All specifications are subject to change without notice. CEVA-TeakLite, CEVA-TeakLite-II, CEVA-Teak, Xpert-Teak, Xpert-TeakLite-II, CEVA-XS, CEVA-Audio, CEVA-VoP, Mobile-Media1000, Mobile-Media2000, PineDSPCore, OakDSPCore, TeakLite, PalmDSPCore are trademarks or registered trademarks of CEVA, Inc. Other company and product names mentioned in this document may be the trademark or registered trademark of their respective manufacturers

Disclaimer: the information is provided "as is" without any express or implied warranty of any kind including warranties or merchantability, non-infringement of intellectual property, or fitness for any particular purpose. In no event shall CEVA, Inc. or its suppliers be liable for any damages whatsoever arising out of the use of or inability to use the materials. CEVA, Inc. and its suppliers further do not warrant the accuracy or completeness of the information, text, graphics or other items contained within these materials. CEVA, Inc. may make changes to these materials, or to the products described within.