



CEVA-TeakLite

CEVA-TeakLite Target Markets

- Cellular handsets
 - 2G – GSM, CDMA, TDMA
 - 2.5G – GPRS, EDGE
- Portable audio (MP3/AAC players)
- Voice over IP
- Hard Disk Drives
- Medical (Hearing–Aid)

CEVA’s Licensable DSP Cores

CEVA, Inc. is the world leader licensor of programmable Digital Signal Processor (DSP) Cores and integrated-applications to the semiconductor and electronics industry. CEVA’s product line offers a variety of DSP cores; each core delivers a different balance of performance, power-efficiency and cost-effectiveness to optimize the devices in which they are incorporated.

CEVA-TeakLite™ is the third generation of licensable DSP Cores in the company’s wide range portfolio of leading edge DSP core technology solutions that include the pre-decessor generation line of the CEVA-Oak™ and CEVA-Pine™ preceded by the CEVA-Teak™, CEVA-Palm™ and CEVA-X™ DSP Cores.

Overview

CEVA-TeakLite DSP Core is a low power, single Multiply-Accumulate (MAC), 16-bit, Fixed point DSP Core, designed specifically to be embedded in highly integrated System-on-Chip (SoC) applications. It provides various resources for customization and differentiated configuration such as program and data memory size and type (e.g. RAM, ROM Flash etc), interfaces to DSP related peripherals (DMA, Timer, etc.) and other system interfaces.

CEVA-TeakLite is assembly and binary compatible with its predecessor DSP generation, the widely adopted CEVA-Oak DSP Core, providing leverage on the large installed base of legacy software available for this product and migrate it to higher performance DSP. The CEVA-TeakLite Core has an advanced set of Digital Signal Processing instructions as well as general microprocessor functions. The Core's programming model and instruction set are designed for straightforward generation of efficient and compact code composed of 16-bit width instructions.

CEVA-TeakLite supports access to 64K-word program memory and can efficiently handle large programs that are needed when the DSP is used for both DSP and control functions. Dedicated mechanisms are implemented supporting real-time operating systems, such as unlimited nesting levels of zero-overhead mechanisms (Block-Repeat and the Repeat instructions) and wide Automatic Context Switching.

CEVA-TeakLite is fully synthesizable (Soft Core), process independent design, allowing the customer to select the optimal operating point in terms of silicon area, power consumption and frequency. A complete DSP solution, supported by a wide range of deliverables, is offered for significantly reducing customer's time-to-market. The deliverables include complete and fully automated reference design implementation along with a verification & simulation environments. CEVA-TeakLite design can be ported to an FPGA for prototyping and system integration. In addition, complete set of Hardware and Software development tools are delivered for highly efficient development of the customer's product. CEVA-TeakLite is backed up by wealthy software and algorithms support available by CEVA's 3rd parties network. A design service is offered for delivering the Core as a Hard-macro to be utilized as part of the user's custom chip.

Architecture Highlights

- › High frequency – up to 190 MHz @ 0.13μ worst case process
- › Low power consumption
 - Active mode – using full DSP capability
 - Slow mode – clock speed and current consumption, linearly divided, relative to active mode by a user-defined factor
 - Stop mode – leakage current only
- › High code density using 16-bit instructions width

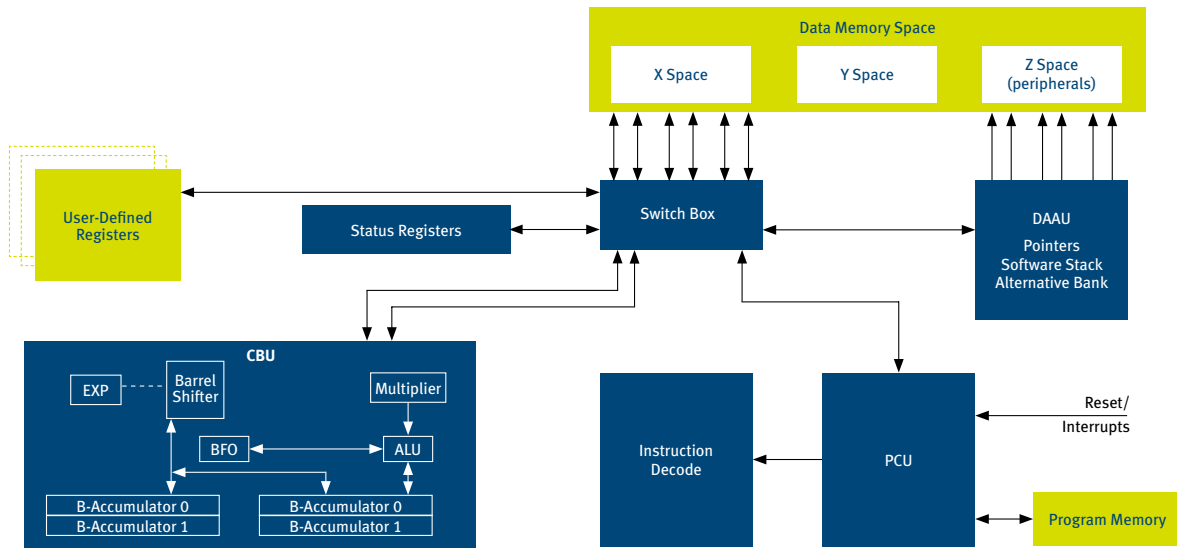
Note: Frequency depends on configuration, synthesis, foundry, process, operating conditions and libraries.

Computation and Bit Manipulation Unit (CBU)

- › 16x16-bit multiplier
 - Multiply-Accumulate (MAC) in a single cycle
 - Double precision multiplication
- › Two parallel 16-bit transfers to/from data memory
- › 36-bit Arithmetic Logic Unit (ALU)
- › Four independent 36-bit accumulators
- › Automatic saturation on overflow
- › Bit Field Operations support
- › 36-bit barrel-shifter
- › Exponent unit for single cycle exponent evaluation
- › Full normalization in a single cycle
- › Maximum/Minimum single cycle instruction with pointer latching
- › Single cycle division step support

Data Address and Arithmetic Unit (DAAU)

- › Data memory addressing modes:
 - Indirect
 - Short/Long Direct
 - Short/Long Index
 - Bit-reverse
 - Stack Pointer
- › Six 16-bit general-purpose address pointer registers
- › Enables both linear and cyclic pointer modification
- › Index base register
- › Stack pointer register
- › Alternative bank of registers
- › Enables two 16-bit data memory transactions in parallel
- › Generates three sets of busses and controls to data memory



CEVA-TeakLite Block Diagram

- › Supports access to four User Defined Registers for hardware accelerators

Program Control Unit (PCU)

- › Pipeline breaks and exceptions handling
- › Zero Overhead looping
 - Block repeat
 - Repeat instruction
- › Single cycle interrupt latency with interrupt context-switching support
- › Interrupts types
 - Three maskable
 - Non-maskable
 - Breakpoint (hardware interrupt)
 - Trap (software interrupt)
- › Code downloading support
- › Program ROM protection

Memory Organization

- › Program memory space
 - Up to 64K-word
- › Data memory space
 - 64K-word size, divided into three sections
 - X & Y spaces – for zero wait-state transactions
 - Z space – for slow devices
 - Flexible configuration of the three spaces (1K-word resolution)

Software Development Tools

The CEVA-TeakLite is accompanied by the advanced Integrated Development Environment (IDE) based Software Development Tools for embedded applications, supporting Windows and Solaris operating systems.

- › IDE Features
 - Project management
 - Makefile generation
 - Tools/project settings
 - Complete tools connectivity
 - Source control connectivity
 - Fully featured editor
 - Browsing information
 - Online help
- › Highly optimizing C and C++ Compiler
 - High-end optimization exploiting the Core’s architecture for efficient code generation
- › Macro Assembler and Linker
 - Architectural restrictions checking and errors overcoming mechanism
 - Advanced mapping mechanism (Auto, Semi-auto and Manual)
 - Section overlay and multi-paging support
- › Advance Graphic User Interface Debugger
 - Simulation and emulation support (same look & feel)
 - Source level debugging support – C/C++ and assembly files
 - User customizable DLLs for Debugger adaptation (Simulator extension, HW interface, etc.)

- Parallel port, USB and JTAG emulation interfaces
- Run-time violation detection by the simulator
- Extensive breakpoint support, interrupt simulation and I/O support
- Tight MATLAB Bi-Directional connectivity
- Integrated graphic application Profiler

- › Various Utilities and Converters
 - Libraries generation
 - Produce various memory burnable formats

Hardware Development Tools

CEVA-TeakLite Development Chip

The development chip is used for emulating TeakLite based systems. It is a RAM-based version and gives all development capabilities needed. The development chip includes:

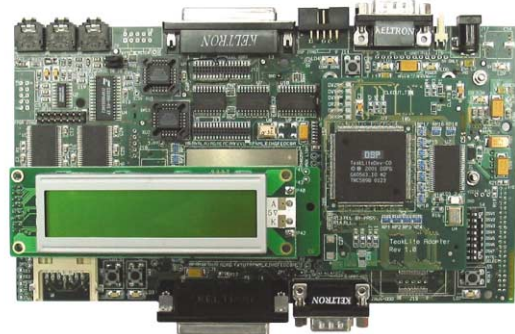
- › 64K-word Program RAM
- › 32K-word Data RAM
- › On-chip Emulation
- › JTAG Support
- › Interrupts control
- › Boot routine
- › General Purpose I/Os
- › User Defined Registers

CEVA-TeakLite Evaluation and Development Platform

The Evaluation and Development Platform (EDP) is used for CEVA-TeakLite based application development. The EDP interfaces to a host PC through the JTAG interface (JBox) for full application control and contains the following:

- › Memories
 - 128M-byte SDRAM memory
 - 256K-byte Flash memory
 - 512K-byte external program memory (expansion card)
 - 1M-byte X&Y external data memory (expansion card)
- › FPGA controller
- › LCD display connector
 - Parallel port interface
 - UART interface
- › Stereo interface
 - Speakers
 - Line in
 - Microphone
- › Multimedia card slot

CEVA-TeakLite Evaluation and Development Platform



Core Module Base Platform

The DSP Core Module Base Platform (CMBP) is a development board that is used to support the development of applications and hardware for CEVA's cores. The CMBP can be connected to ARM's Integrator development system, thus allowing the user to develop ARM+DSP based applications. In addition, the CMBP provides hardware support for multi-core debugging (e.g. ARM).

Emulation Board

The Emulation Board (EB) is a small form factor board that includes the CEVA-TeakLite silicon chip and JTAG interface functions. It is mainly used for the development of pure real time DSP algorithms and as a starter kit for evaluation purposes.

CEVA-TeakLite on FPGA

A dedicated tool that allows FPGA implementation of the CEVA-TeakLite. The user can build an FPGA emulation model of the SoC containing the CEVA-TeakLite and additional components, in order to verify the design before taping out the actual silicon.

DBGVerifier

The DBGVerifier is a tool that allows the CEVA-TeakLite Debugger to connect to the DSP core HDL implementation on the Verilog simulator. The connection to the Verilog simulator enables the user to test the HDL implementation of the DSP core, check the JTAG interface, load and execute small programs and make sure that the system can enter emulation mode without problems. The DBGVerifier increases the level of confidence before tape-out and provides the user with another way to verify the accuracy of the design.

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