



CEVA-TeakLite-II

CEVA-TeakLite-II Target Markets

- › Cellular handsets
 - 2G – GSM, CDMA, TDMA
 - 2.5G – GPRS, EDGE
- › Portable Media Players
- › Voice over IP / Voice over WLAN
- › Hard Disk Drives
- › Optical Disk Servo Control
- › Portable Audio Devices

CEVA’s Licensable DSP Cores

CEVA, Inc. is the world leader licensor of programmable Digital Signal Processor (DSP) Cores and integrated-applications to the semiconductor and electronics industry. CEVA’s product line offers a variety of DSP cores; each core delivers a different balance of performance, power-efficiency and cost-effectiveness to optimize the devices in which they are incorporated.

CEVA-TeakLite-II™ is a licensable DSP Core in the company’s wide range portfolio of leading edge DSP core technology solutions that include the predecessor generation line of the CEVA-TeakLite™, CEVA-Oak™ and CEVA-Pine™ preceded by the CEVA-TeakLite-III™, CEVA-Teak™ and CEVA-X™ DSP Cores.

Overview

CEVA-TeakLite-II DSP Core is a low power, single Multiply-Accumulate (MAC), 16-bit fixed point DSP core, designed specifically to be embedded in highly integrated System-on-a-Chip (SoC) designs. At a speed of 245MHz (90nm worst case), the TeakLite-II performance, cost and power presents an attractive metric that is applicable to emerging high volume in the consumer and in wireless markets.

CEVA-TeakLite-II Core has an advanced set of Digital Signal Processing instructions as well as general microprocessor functions. The Core's programming model and instruction set are designed for straightforward generation of efficient and compact code composed of 16-bit instruction width. TeakLite-II integrates run time debug functionality useful for field updates and remote fault detections and supports various memory configurations and system peripherals such as DMA, Timers, Serial Ports and bus bridges.

CEVA-TeakLite-II supports access to 1M word program memory and can efficiently handle large code sections, required when the DSP is used for both digital signal processing and control functions. The DSP can also handle and process large data buffers, accessing up to 1M word data memory space.

CEVA-TeakLite-II is binary compatible with its predecessor DSP generations, the widely adopted CEVA-TeakLite and CEVA-Oak DSP Cores, allowing its users to leverage on the existing applications and large installed base of software available for these products and easy migrate it to higher performance DSP.

CEVA-TeakLite-II is a fully synthesizable (Soft Core), process independent design, allowing the customer to select the optimal operating point in terms of silicon area, power consumption and frequency.

A complete DSP solution, supported by a wide range of deliverables, is offered for significantly reducing customer's time-to-market. The deliverables include complete and fully automated reference design implementation along with a verification & simulation environments. CEVA-TeakLite-II design can be ported to an FPGA for prototyping and system integration.

In addition, a complete set of Software development tools are delivered for highly efficient development of the customer's product. CEVA-TeakLite-II is backed up by a wide variety of software, applications and algorithms support available by CEVA and CEVAnet third-party community. Design services are also offered, for example delivering the Core as a Hard-macro to be utilized as part of the user's custom chip.

Architecture Highlights

- › 16-bit fixed point, single MAC DSP core
- › High frequency – 245 MHz @ 90nm process, worst case*
- › Very small DSP engine footprint – 0.24 mm² @ 90nm*
- › Low power consumption
 - Active mode – using full DSP capability
 - Slow mode – clock speed and current consumption, linearly divided, relative to active mode by a user-defined factor
 - Stop mode – leakage current only
- › High code density using 16-bit instructions width
- › Embedded (optional) On-Chip Emulation (OCEM) and JTAG modules
- › Memory space
 - Up to 1M word addressable program space
 - Up to 1M word addressable data space

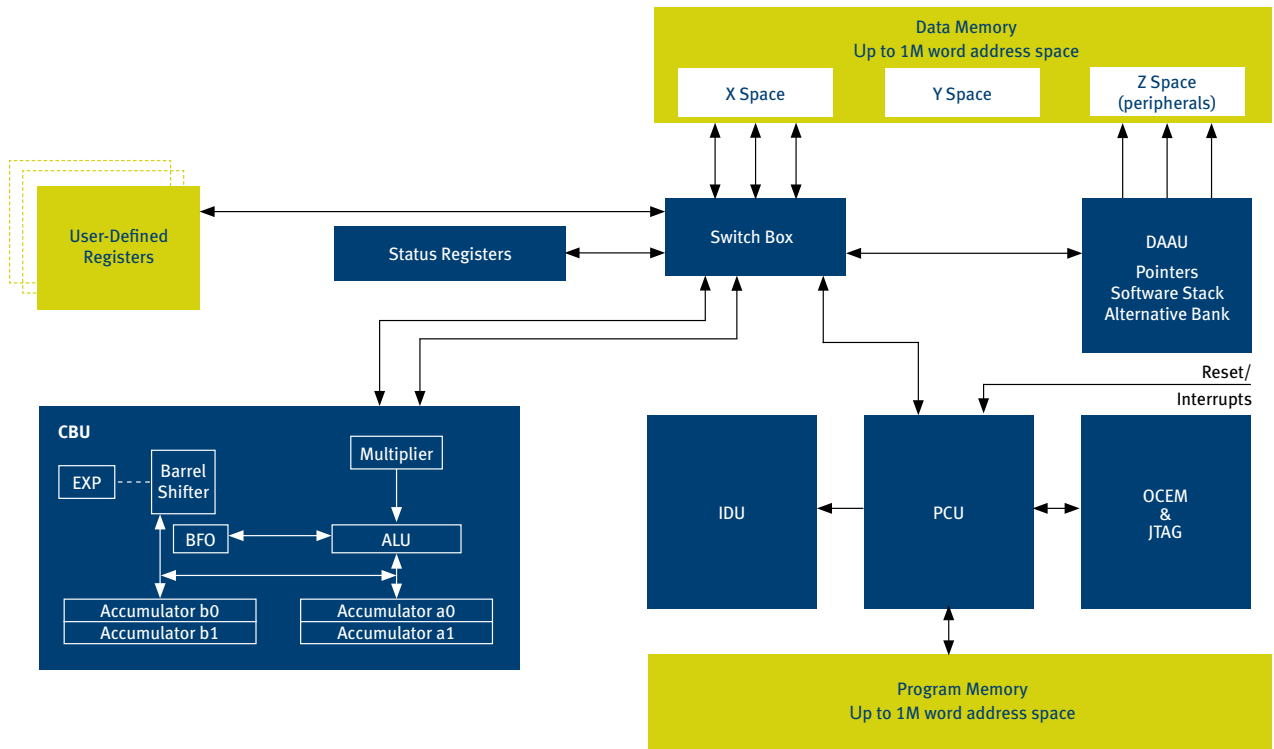
Computation and Bit Manipulation Unit (CBU)

- › 16x16-bit multiplier
 - Multiply-Accumulate (MAC) in a single cycle
 - Double precision multiplication support
- › Two parallel 16-bit transfers to/from data memory
- › 36-bit Arithmetic Logic Unit (ALU)
- › Four independent 36-bit accumulators
- › Automatic saturation on overflow
- › Bit Field Operations: Set, Reset, Change and Test. Executed directly on registers and data memory content, with no affect on accumulators' content.
- › 36-bit barrel-shifter
- › Single cycle exponent evaluation of up to 36-bit values
- › Full normalization in a single cycle
- › Single cycle data move & shift capability
- › Maximum/Minimum single cycle instruction with pointer latching
- › Single cycle division step support

Data Address and Arithmetic Unit (DAAU)

- › Data memory addressing modes:
 - Indirect
 - Short/Long Direct
 - Short/Long Index
 - Bit-reverse
 - Stack Pointer

* **Notes:** Frequency depends on configuration, synthesis, foundry, process, operating conditions and libraries; Significantly smaller footprint can be achieved when targeting lower frequency.



CEVA-TeakLite-II Block Diagram

- > Six 16-bit general-purpose address pointer registers
- > Enables both linear and cyclic pointer modification
- > Index base register
- > Stack pointer register
- > Alternative bank of registers
- > Enables two 16-bit data memory transactions in parallel
- > Generates three sets of busses and controls to data memory
- > Supports access to four User Defined Registers for hardware accelerators

Program Control Unit (PCU)

- > Pipeline breaks and exceptions handling
- > Zero Overhead looping by two interruptible mechanisms:
 - Four nesting levels of Block repeat
 - Single instruction Repeat

- > Interrupts:
 - Three maskable
 - One non-maskable
 - Breakpoint (hardware interrupt)
 - Trap (software interrupt)
- > Code downloading support
- > Program ROM protection

Memory Organization

- > Program memory space
 - Up to 1M word (using paging)
- > Data memory space
 - Up to 1M word (using paging), divided into three sections
 - X & Y spaces – for zero wait-state transactions
 - Z space – for slow devices
 - Flexible configuration of the three spaces (1K-word resolution)

Development Tools

Software Development Tools

The CEVA-TeakLite-II is accompanied by the advanced Integrated Development Environment (IDE) based Software Development Tools for embedded applications, supporting Windows, Solaris and Linux operating systems.

IDE Features

- › Project management
- › Makefile generation
- › Tools/project settings
- › Complete tools connectivity
- › Source control connectivity
- › Fully featured editor
- › Browsing information
- › Assembly syntax tips and auto completion
- › Online help

Highly optimizing C and C++ Compiler

- › High-end optimization exploiting the Core's architecture for efficient code generation
 - Tight control on the Compiler's code generation
 - Supporting mechanisms for mixing C/C++ and Assembly

Macro Assembler and Linker

- › Architectural restrictions checking and errors overcoming mechanism
- › Advanced mapping mechanism (Auto, Semi-auto and Manual linking)
- › Section overlay and multi-paging support

Advance Graphic User Interface Debugger

- › Simulation and emulation support (same look & feel)
- › Source level debugging support - C/C++ and assembly files
- › User customizable DLLs for Debugger adaptation (Simulator extension, HW interface, etc.)
- › Parallel port, USB and JTAG emulation interfaces

- › Run-time violation detection by the simulator
- › Extensive breakpoint support, interrupt simulation and I/O support
- › Tight MATLAB Bi-Directional connectivity
- › Integrated graphic application Profiler

Various Utilities and Converters

- › Libraries generation
- › Produce various memory burnable formats

CEVA-TeakLite-II on FPGA

A dedicated tool that allows FPGA implementation of the CEVA-TeakLite-II. The user can build an FPGA emulation model of the SoC containing the CEVA-TeakLite-II and additional components, in order to verify the design before taping out the actual silicon.

DBGVerifyer

The DBGVerifyer is a tool that allows the CEVA Debugger to connect to the DSP core HDL implementation on the Verilog simulator. The connection to the Verilog simulator enables the user to test the HDL implementation of the DSP core, check the JTAG interface, load and execute small programs and make sure that the system can enter emulation mode without problems. The DBGVerifyer increases the level of confidence before tape-out and provides the user with another way to verify the accuracy of the design.

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