



## CEVA-TeakLite-III

### CEVA-TeakLite-III Target Markets

- › **HD Audio Applications:** Digital TVs, HD-DVDs, Blu-ray Discs, Set-top Boxes, A/V Receivers, IPTV
- › **Low-cost Mobile Handsets:** 2G/2.5G/3G baseband, wideband voice codecs, audio codecs and post-processing
- › **Music-Centric Mobile Handsets:** supporting advanced audio use cases
- › **VoIP Gateways:** Up to 10 channels, including VoIP codecs (e.g. G.723.1), echo cancellation, DTMF generation and detection, networking functions
- › **Portable Media Player (PMP):** 5.1 channel audio processing
- › **Dual-Mode Cellular / VoWiFi Handsets**
- › **Next-Generation Disk Drives:** Servo control and dual-layer optical disks, HDDs, HD-DVD, Blu-ray Disc

### CEVA's Licensable DSP Cores

CEVA is the leading licensor of digital signal processor (DSP) cores, multimedia and storage platforms to leading semiconductor and OEMs worldwide. CEVA's product line includes a variety of DSP cores; each core delivers a different balance of performance, power-efficiency and cost-effectiveness, optimized for different applications.

CEVA-TeakLite-III™ is the successor of the CEVA-Teak™ CEVA-TeakLite™ and CEVA-TeakLite-II™ DSP cores, the most established and licensed DSPs in the industry. By offering full compatibility to its predecessors, the CEVA-TeakLite-III leverages on the extensive customer-base of its predecessors and allows a seamless migration path for existing applications and System-on-Chips (SoCs).

### Overview

CEVA-TeakLite-III is a low power, dual Multiply-Accumulate (MAC), 32-bit fixed point DSP core, specifically designed to be embedded into highly integrated SoCs. Running at speeds

higher than 650MHz in 65nm (worst-case conditions), the CEVA-TeakLite-III offers a significant enhancement over its predecessors, enabling licensees to easily meet advanced application requirements and use-cases, including HD Audio, multi-mode low-cost wireless handsets, multi-channel VoIP gateways, and dual-mode cellular/VoWiFi phones.

Various 32-bit processing functions, inherent to the CEVA-TeakLite-III, further enhance its performance and quality for HD Audio applications and codecs, many of which require 32-bit precision calculations. A 64-bit data memory bandwidth ensures the DSP can be constantly fed with data samples and coefficients for continuous processing.

In order to ease the application porting process into the CEVA-TeakLite-III, the DSP also combines numerous RISC-oriented features, including a linear 4GB memory space, enabling the porting of large applications while eliminating the overhead of paging data and instructions. A cached memory subsystem and optional memory management and protection mechanisms significantly reduce the application development effort, avoiding the management of memory segments in software and allowing true multi-tasking applications to efficiently run with an RTOS.

The CEVA-TeakLite-III combines two types of instruction sets: CEVA-Quark™, a complete set of 16-bit instructions, targeted at reducing memory size and die cost (see sidebar); and an advanced set of 32-bit instructions, useful for the most processing-hungry sections of the application. Application developers can freely mix instructions from both sets, without the need to switch modes, enabling to balance performance versus cost.

CEVA-TeakLite-III is a fully synthesizable (Soft Core) process independent design, allowing the customer to select the optimal operating point in terms of silicon area, power consumption and frequency, and port it to any foundry and process.

## CEVA-TeakLite-III – A Powerful DSP Core for HD Audio Applications

Processing requirements for high-end audio applications are evolving dramatically, requiring a dedicated and powerful programmable engine. Decoding of multiple audio streams simultaneously has become a standard requirement for next generation HiFi devices, multiplying the necessary processing horsepower. Each of those streams could use 7.1 channels, adding 2 channels to the existing 5.1 channels typical in existing devices.

### CEVA-Quark

CEVA-Quark™ is a stand-alone comprehensive Instruction Set Architecture (ISA) embedded into the CEVA-TeakLite-III. This unique ISA is targeted at reducing die size and die cost, by utilizing only 16-bit instructions. This further reduces power consumption, having fewer memory accesses.

CEVA-Quark ISA represents a complete set of instructions, including:

- Memory accesses
- Arithmetic and multiplication operations
- Logical, shift and bit manipulation instructions
- Control operations

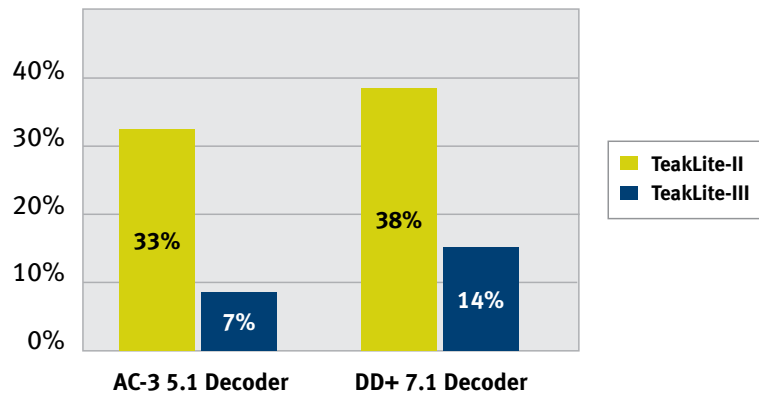
Application developers can mix CEVA-Quark instructions with other, more advanced CEVA-TeakLite-III instructions, without a need to switch to different modes. The CEVA-TeakLite-III compiler can be switched to optimize the generated code to minimum code size, utilizing the CEVA-Quark ISA as much as possible.

In addition, a dozen new HD Audio standards are being deployed in most next generation devices, including Dolby Digital Plus, Dolby TrueHD, DTS-HD and Dolby MLP. The wealth of standards calls for a programmable engine, such as a DSP, while the increased complexity and hi-fidelity requirements demand a powerful 32-bit engine for the task.

The CEVA-TeakLite-III is a true 32-bit DSP running at 700MHz and perfectly fits such advanced applications. Other enhancements such as a FFT and Huffman accelerators and powerful audio-specific instructions reduce the overall MHz requirements for the CEVA-TeakLite-III when dealing with advanced HD Audio codecs.

The diagram below demonstrates the enhanced capabilities of the CEVA-TeakLite-III running HD Audio codecs, such as AC-3 5.1 channels and Dolby Digital Plus 7.1 channels. For instance, only 14% of the total available MHz of the DSP (at 90nm process) are required to decode a Dolby Digital Plus 7.1 channel stream, which allows the core to simultaneously decode 4 such streams with enough headroom for other post-processing functions.

Percentage of maximum DSP MHz



### CEVA-TeakLite-III Enhancements Over Predecessors

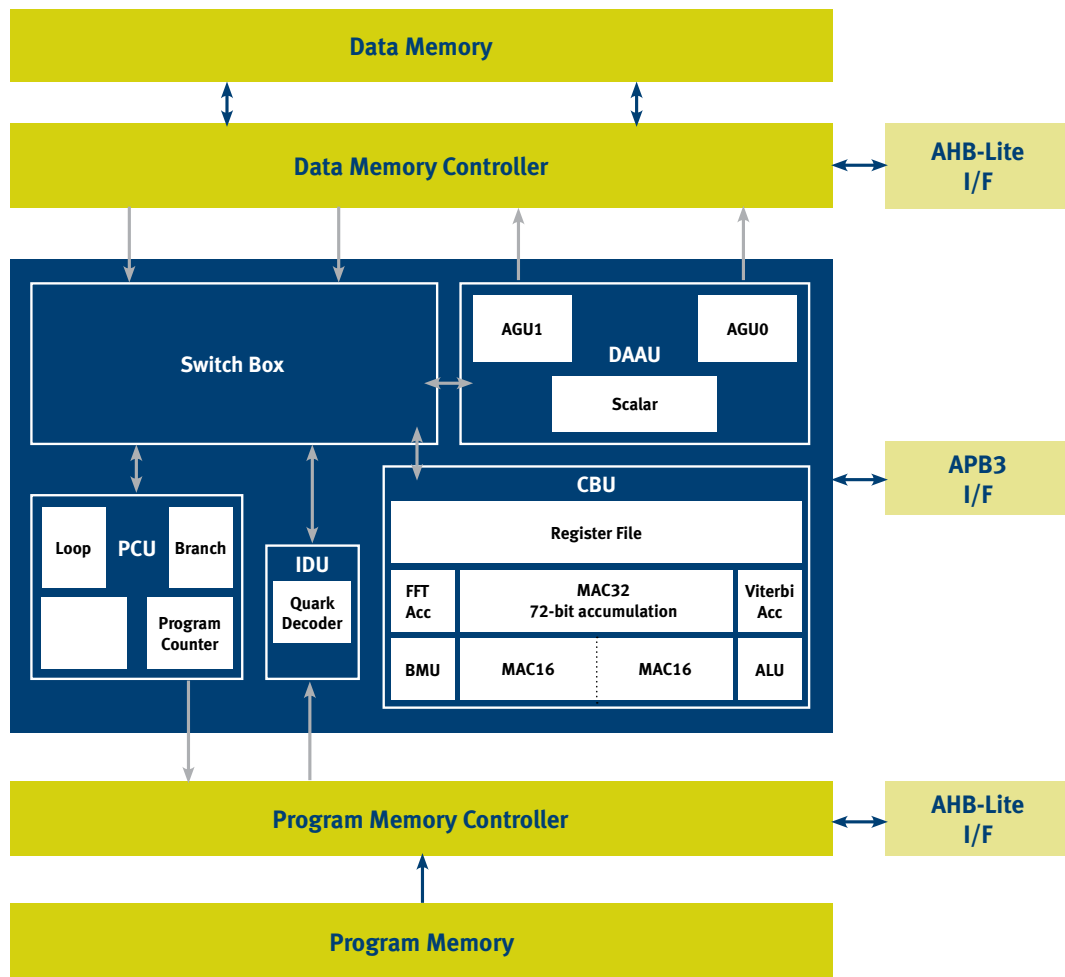
While CEVA-TeakLite-III maintains full backward compatibility with its predecessors – the CEVA-TeakLite and CEVA-TeakLite-II – it includes some major enhancements in its architecture and micro-architecture.

CEVA-TeakLite-III Architecture Enhancements

| Parameter                         | TeakLite                    | TeakLite-II   | TeakLite-III                            |
|-----------------------------------|-----------------------------|---|---|
| Max Frequency @ 90nm <sup>1</sup> | 200                         | 245   | 400                                     |
| Pipeline stages                   | 4                           | 4   | Variable, up to 10                      |
| 32-bit MAC unit                   | No                          | No  | Yes                                     |
| 16-bit multiplications            | Single                      | Single  | Dual                                    |
| Parallel Instructions             | No                          | No  | Yes                                     |
| Instruction Predication           | No                          | No  | Yes                                     |
| Memory Space                      | Program: 64KW<br>Data: 64KW | Program: Multiple 64KW pages<br>Data: Multiple 64KW pages | Program: Linear 4GB<br>Data: Linear 4GB |
| Loop nesting levels               | Up to 4                     | Up to 4   | Infinite                                |
| FFT and Viterbi Acceleration      | No                          | No  | Yes                                     |
| Accumulators                      | 2 + 2 auxiliary             | 2 + 2 auxiliary   | 4 orthogonal accumulators               |
| Pointers                          | 6 x 16-bit                  | 6 x 16-bit  | 8 x 32-bit                              |

1 – Frequency is at worst-case conditions

CEVA-TeakLite-III Block Diagram



## CEVA-TeakLite-III Architecture Highlights

### General

- › 32-bit fixed point DSP
- › Dual 16-bit MAC, single 32x32-bit MAC with 72 bit accumulation
- › Backward compatible with predecessors – CEVA-TeakLite and CEVA-TeakLite-II
- › High frequency\* – over 400 MHz @ 90nm process; 700MHz @ 65nm process
- › Small die size – only 0.4sqmm in 90nm process
- › Low power consumption – 0.1 mW/MHz @ 90nm process, for typical processing load
- › Variable length pipeline, up to 10-stages, enabling high-speed design with slow memories
- › Supports 4GB linear memory space, eliminating any paging overhead
- › Variable instruction width – mix of 16-bit instructions (CEVA-Quark™) for code density, and 32-bit instructions for high performance
- › Supports SIMD operations, further enhancing ILP and code density
- › Includes accelerators for key algorithms – FFT, Viterbi and Huffman coding

### RISC-Oriented Features

Enable Easy and Efficient SW Porting into the CEVA-TeakLite-III Core

- › 4GB (32-bit) linear address space
- › Unified set of 32-bit registers, for general purpose processing
- › 32-bit scalar unit, executes most arithmetic, logical, shift and bit manipulation operations in a single cycle using the unified register bank
- › Cached memory subsystem, eases the application development process
- › Memory management and protection capabilities, useful for multi-tasking OS-based applications
- › Branch prediction mechanism, shortening branch latencies down to a single cycle
- › Quick look-up-table (LUT) access, efficient for memory-based decision making processing
- › Predicated execution – most instructions can be executed conditionally, eliminating most branch instructions and improving cycle count and code size

### High Efficiency for Advanced DSP Processing

- › Dual 16-bit MAC, including scaling and saturation
- › Single 32x32 bit MAC, with multiple scaling options
- › Filter processing acceleration, using dedicated

connectivity between both 16-bit MACs

- › 16-bit SIMD operations
- › 64-bit memory bandwidth, ensure DSP can be fed with data continuously
- › Four orthogonal accumulators
- › Supports parallel instructions – up to 3 instructions simultaneously
- › Viterbi acceleration – 2 cycles per ACS (add-compare-select) operation
- › FFT acceleration (single and double precision) – 2 cycle per 16-bit butterfly, 4 cycles per 32-bit double precision butterfly

### Powerful Memory Addressing Capabilities

- › Generates two independent 32-bit data addresses each cycle
- › Supports a wide variety of addressing modes, including:
  - Indirect
  - Indexed (useful for table accesses)
  - Bit-reverse (beneficial for FFT)
  - Direct
  - SW stack
- › Linear memory space (as opposed to X/Y), guarantees efficient out-of-the-box C compilation
- › Parallel instructions support storing previous results to memory
- › Round and store operations
- › 64-bit memory access to stack memory, allows quick context switching
- › Includes a 32-bit integer unit (scalar) for address manipulation and general purpose processing

### Multi-Tasking Enabled System

- › Optional memory management and protection features
- › Multiple interrupt sources, including maskable, non-maskable and vectored interrupts
- › Unlimited nesting levels of loops
- › Fast context switching

### Advanced Memory Configurations

The CEVA-TeakLite-III core is equipped with a complete memory subsystem (MSS):

- A configurable L1/L2 memory organization including: TCM, caches, system peripherals and system interfaces
- Ensures easy integration into target SoC
- Allows licensees to balance performance with die size

\* **Notes:** Frequency depends on configuration, synthesis, foundry, process, operating conditions and libraries; Significantly higher frequency can be achieved under different conditions and libraries.

## Software Development Tools

The CEVA-TeakLite-III is accompanied by the advanced Integrated Development Environment (IDE) based Software Development Tools for embedded applications, supporting Windows, Linux and Solaris operating systems.

### IDE Features

- Project management
- Makefile generation
- Tools/project settings
- Complete tools connectivity
- Source control connectivity
- Fully featured editor
- Browsing information
- Assembly syntax tips and auto completion
- Online help

### Highly optimizing C and C++ Compiler

- High-end optimization exploiting the core's architecture for efficient code generation
- Tight control on the Compiler's code generation
- Supporting mechanisms for mixing C/C++ and Assembly

### Macro Assembler and Linker

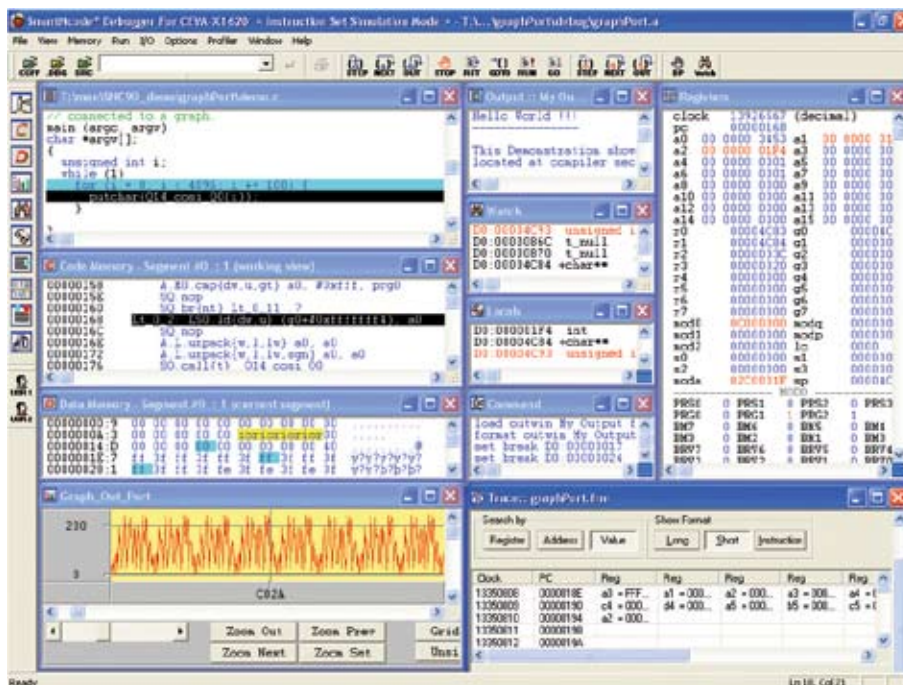
- Architectural restrictions checking and errors overcoming mechanism
- Advanced mapping mechanism (Auto, Semi-auto and Manual linking)
- Section overlay and multi-paging support

### Advance Graphic User Interface Debugger

- Cycle Accurate and Instruction Set Simulation of the core and memory sub system
- Emulation support (same look & feel as simulation)
- Source level debugging support - C/C++ and assembly files
- User customizable DLLs for Debugger adaptation (Simulator extension, HW interface, etc.)
- Parallel port, USB and JTAG emulation interfaces
- Run-time violation detection by the simulator
- Extensive breakpoint support, interrupt simulation and I/O support
- Tight MATLAB Bi-Directional connectivity
- Integrated graphic application Profiler

### Various Utilities and Converters

- Libraries' generation
- Produces various memory burnable formats



Debugger Screen View





 [www.ceva-dsp.com](http://www.ceva-dsp.com)



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