



**CEVA-Teak**

**CEVA-Teak Target Markets**

- › 2.5G/3G Cellular handsets
  - Base-band
  - Application processing
- › PDAs and Smart phones
- › VoIP
  - Handset terminals
  - IP phones
  - Gateways
- › Portable Audio
- › Digital Still Camera

**CEVA's Licensable DSP Cores**

CEVA, Inc. is the world leader licensor of programmable Digital Signal Processor (DSP) Cores and integrated-applications to the semiconductor and electronics industry. CEVA's product line offers a variety of DSP cores; each core delivers a different balance of performance, power-efficiency and cost-effectiveness to optimize the devices in which they are incorporated.

CEVA-Teak™ is the fourth generation of licensable DSP Cores in the company's wide range portfolio of leading edge of DSP core technology solutions. This portfolio includes the predecessor generation line of the CEVA-TeakLite™, CEVA-Oak™ and CEVA-Pine™ preceded by the advanced products of the CEVA-Palm™ and the CEVA-X™ DSP Cores.

## Overview

CEVA-Teak DSP Core is a low power, high performance, dual Multiply-Accumulate (MAC), 16-bit, Fixed-point DSP core, designed specifically to be embedded in highly integrated System-on-Chip (SoC) applications. CEVA-Teak provides interface to program and data memories of different size and type as well as interfaces to DSP related peripherals, such as Interrupt and Power management controllers

CEVA-Teak is binary compatible with the CEVA-TeakLite and CEVA-Oak DSP Cores, providing leverage on the large installed base of legacy software available for these products. The CEVA-Teak Core has a powerful set of DSP instructions as well as general microprocessor Functions. The Core's programming model and instruction set are designed for straightforward generation of efficient and compact code composed of 16-bit width instructions in addition to a sub-set of parallel instructions.

CEVA-Teak supports access to 4M-word program memory and can efficiently handle very large programs that are needed when the DSP is used for both DSP and massive control functions. Dedicated mechanisms were added to support real-time operating systems, such as unlimited nesting levels of zero-overhead mechanisms (Block-Repeat and Repeat) and advanced Context Switching capability.

CEVA-Teak is fully synthesizable (Soft Core), process independent design, allowing the customer to select the optimal operating point in terms of silicon area, power consumption and frequency. A complete DSP solution, based on the CEVA-Teak range of deliverables, is offered for reducing customer's time-to-market significantly. The deliverables include complete and fully automated reference design implementation along with a verification & simulation environments. Additionally, CEVA-Teak is available as a Hard-macro to be utilized as part of the user's custom chip design. The Core is offered also with peripherals (fully implemented in the XpertTeak™), system interface modules, FPGA design flow and other components providing a full DSP solution. Additionally, CEVA-Teak is backed up by wealthy software and algorithms support available by CEVA's 3rd parties network. In addition, complete set of Hardware and Software development tools are delivered for highly efficient software and hardware development of the customer's product.

## Architecture Highlights

- › High frequency - up to 160MHz @ 0.13μ worst case process
- › Low power consumption
  - Active mode - using full DSP capability
  - Slow mode - Clock speed and current consumption, linearly divided, relative to active mode by a user-defined factor
  - Stop mode - Leakage current only
- › Parallel instructions execution capability
- › High code density
  - 16-bit coding

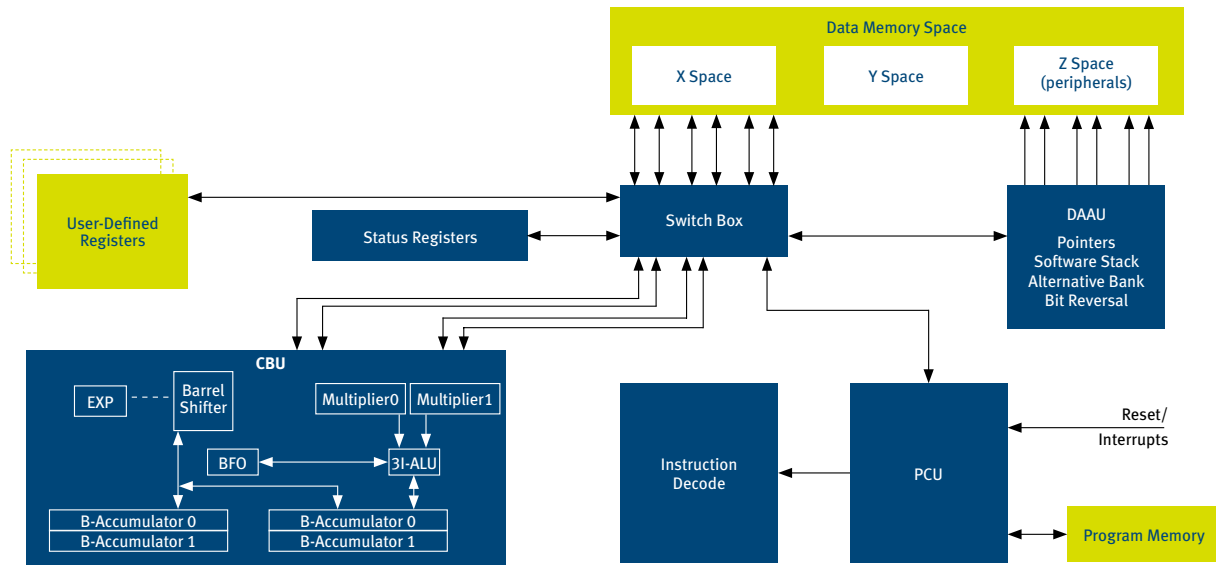
**Note:** Frequency depends on configuration, synthesis, foundry, process, operating conditions and libraries

### Computation and Bit Manipulation Unit (CBU)

- › Two 16x16 bits multipliers
  - Dual Multiply-Accumulate (MAC) in a single cycle
  - Double precision multiplication
- › Four parallel 16-bit transfers from data memory
- › Full normalization operation in two cycles
- › 40-bit Arithmetic Logic Unit (ALU)
  - 3 Input ALU
  - Split ALU
- › Floating point support with single cycle exponent evaluation
- › Bit extract support (e.g. GSM)
- › 40-bit barrel shifter (left and right)
- › Four independent 40-bit accumulators
  - Partitioned into – 2x16 bits + 8 guard bits
  - Store/Restore 32-bit accumulator part in a single cycle
  - Shadow accumulators
- › Saturation of 32-bit operations
- › Single cycle division step
- › Viterbi built in accelerator
- › Maximum/Minimum single cycle instruction with pointer latching and modification
- › Dedicated FFT accelerator – 5 cycles butterfly calculation
- › Viterbi built in accelerator – 3 cycles for two add compare-select in

### Data Address and Arithmetic Unit (DAAU)

- › Generates six sets of busses and controls to data memory
- › Range of Data memory addressing modes:
  - Indirect
  - Short/Long Direct



**CEVA-Teak Block Diagram**

- Short/Long Index
- Bit-reverse
- Stack Pointer
- › Enables both linear and cyclic pointer modification
- › Enables four 16-bit data memory transactions in parallel
- › Eight 16-bit general purpose address pointer registers
- › Alternative bank of registers
- › Supports access to four User Defined Registers for HW accelerators

**Program Control Unit (PCU)**

- › Zero Overhead looping
  - Block repeat
  - Repeat instruction
- › Single cycle interrupt latency with Interrupt context switching support
- › Interrupts types:
  - Three maskable
  - Non-maskable
  - Vector
  - Breakpoint
  - Trap (software interrupts)
- › Code downloading support
- › Program ROM protection

**Memory Organization**

- › Program memory space
  - Linear space – up to 256K-word

- Total space paging – up to 4M-word
- › Data memory space
  - 64K-word size, divided into three sections
  - X & Y spaces – for zero wait state transactions
  - Z space – for slow devices
  - Flexible configuration of the three spaces (1K-word resolution)

**Software Development Tools**

The CEVA-Teak is accompanied by the advanced Integrated Development Environment (IDE) based Software Development Tools for embedded applications, supporting Windows and Solaris operating systems.

- › IDE Features
  - Project management
  - Makefile generation
  - Tools/project settings
  - Complete tools connectivity
  - Source control connectivity
  - Fully featured editor
  - Browsing information
  - Online help
- › Highly optimizing C and C++ Compiler
  - High-end optimization exploiting the Core’s architecture for efficient code generation
- › Macro Assembler and Linker
  - Architectural restrictions checking and errors overcoming mechanism
  - Advanced mapping mechanism (Auto, Semi-auto and Manual)
  - Section overlay and multi-paging support

- › Advance Graphic User Interface Debugger
  - Simulation and emulation support (same look & feel)
  - Source level debugging support - C/C++ and assembly files
  - User customizable DLLs for Debugger adaptation (Simulator extension, HW interface, etc.)
  - Parallel port, USB and JTAG emulation interfaces
  - Run-time violation detection by the simulator
  - Extensive breakpoint support, interrupt simulation and I/O support
  - Tight MATLAB Bi-Directional connectivity
  - Integrated graphic application Profiler
- › Various Utilities and Converters
  - Libraries generation
  - Produce various memory burnable formats

## Hardware Development Tools

### CEVA-Teak Development Chip

The development chip is used for emulating Teak based systems. It is a RAM-based version and gives all development capabilities needed. The development chip includes:

- › 128k-word on-chip program memory
- › Extended data memory – 2 pages of 64k-word
- › Glueless access to external program and data memories
- › Memory Interface Unit
- › General Purpose I/Os
- › Interrupt Control Unit (ICU)
- › Power Management Unit (PMU)
- › On Chip Emulation Module (OCEM)
- › JTAG & JTAG Activated Module (JAM)
- › Four User Defined Registers

### CEVA-Teak Evaluation and Development Platform

The Evaluation and Development Platform (EDP) is used for CEVA-Teak based application development. The EDP interfaces to a host PC through the JTAG interface (JBox) for full application control and contains the following:

- › Memories
  - 128M-byte SDRAM memory
  - 256K-byte Flash memory
  - 512K-byte external program memory (expansion card)
  - 1M-byte X&Y external data memory (expansion card)
- › FPGA controller
- › LCD display connector
- › Parallel port interface
- › UART interface

- › Stereo interface
  - Speakers
  - Line in
  - Microphone
- › Multimedia card slot

### Core Module Base Platform

The DSP Core Module Base Platform (CMBP) is a development board that is used to support the development of applications and hardware for CEVA's cores. The CMBP can be connected to ARM's Integrator development system, thus allowing the user to develop ARM+DSP based applications (e.g. multi-core debugging).

## CEVA-Teak Evaluation and Development Platform



### Emulation Board

The Emulation Board (EB) is a small form factor board that includes the CEVA-Teak silicon chip and JTAG interface functions. It is mainly used for the development of pure real time DSP algorithms and as a starter kit for evaluation purposes.

### CEVA-Teak on FPGA

A dedicated tool that allows FPGA implementation of the CEVA-Teak. The user can build an FPGA emulation model of the SoC containing the CEVA-Teak and additional components, in order to verify the design before taping out the actual silicon.

### DBGVerifier

The DBGVerifier is a tool that allows the CEVA-Teak Debugger to connect to the DSP core HDL implementation on the Verilog simulator. The connection to the Verilog simulator enables the user to test the HDL implementation of the DSP core, check the JTAG interface, load and execute small programs and make sure that the system can enter emulation mode without problems. The DBGVerifier increases the level of confidence before tape-out and provides the user with another way to verify the accuracy of the design.