CEVA X1 CONTROLS CELLULAR IOT DEVICES

By Mike Demler (October 31, 2016)

Ceva's new X1 is a synthesizable processor core for cellular-connected IoT and wearable devices that use Narrowband IoT (NB-IoT) communications. The X1 has powerful DSP capabilities, but it can also run general-purpose code with Cortex-M–class performance. It is suited to baseband and Layer 2 functions for NB-IoT as well as Bluetooth, LoRa, Wi-Fi, and ZigBee, along with GNSS location. The company announced the new intellectual property (IP) at the 2016 Linley Processor Conference; customers can license it now.

The X1 is similar to previously released members of the Ceva-X family: the X2 and X4 (see *MCR 8/1/16,* "Ceva X2 Controls Multiple PHYs"). Higher-performance modems can run the X1 at up to a 1.5GHz clock frequency in a 16nm process, but low-power IoT devices employ much slower clocks. The X1 mostly comprises a half-portion of the X2's hardware, offering a single scalar processor unit (SPU) instead of two and halving the SIMD width to 32 bits, the memory interface to 64 bits for load and store, and the number of single-cycle 16x16-bit multiply-accumulators (MACs) to two. Eliminating one SPU reduces the VLIW width from five ways to four.

Designers can optionally augment the X1 with a single-precision FPU. Also optional are a maximum 64KB two-way data cache, maximum 256KB four-way instruction cache, and tightly coupled memories (TCMs). The TCM sizes remain the same as in the X2: 256KB for instructions and 512KB for data. The integrated address-control unit (IACU) is equivalent to a memory-protection unit (MPU), controlling access to protected memory regions. The X1 retains the optional dynamic branch prediction of its siblings, although cellular protocol stacks require that feature. It also retains support for an AXI interface, but the new AHB option is more appropriate for small IoT devices. The optional Ceva Connect traffic manager offloads the core by managing data flow to multiple hardware accelerators.

The X1 ISA offers extensions for the Category M1 and Category NB1 standards, which the 3GPP recently completed in its Release 13 specification (see *NWR 8/31/15,* "Low-Rate LTE Delivers IoT WANs"). The baseband functions include Viterbi and turbo encoders as well as channel-state information (CSI). The Layer 2 functions include encryption for the Packet Data Convergence Protocol (PDCP) and Non-Access-Stratum (NAS) layers. Those instructions save area and power compared with hardware accelerators, which are unnecessary for such low-data-rate NB-IoT tasks. An integrated power-savings unit (PSU) delivers further reductions by shutting down idle portions of the core. It supports Category-M1/NB1 power-savings mode (PSM) and extended discontinuous reception (EDRX).

In parallel with LTE Category NB1, the X1 can handle Bluetooth beacons for indoor positioning, GNSS outdoor positioning, sensor fusion, and voice processing. In an example access-tracker design, it runs both LTE Category NB1 to transmit data, including the complete protocol stack, and GNSS to report position. Such a device is idle most of the time, so the modem can shut down while the device records its position then switch modes to transmit that information along with other sensor-fusion data. According to a Ceva simulation, this kind of device can conserve power by running at less than 150MHz.

Running at a higher clock frequency, the X1 supports multimode wireless communications in cellular-equipped smartwatches running Category M1, delivering up to 1Mbps on the downlink. Such devices lack high-end graphics and media-streaming capability, but they need the higher data rate for voice communications. Because standalone watches typically use only one connectivity mode at a time, a single X1 can handle the LTE baseband, switching to Bluetooth or Wi-Fi when necessary.

The X1 works with Ceva's Riviera Waves IP to support 802.11n Wi-Fi (see *MCR 6/29/15,* "Ceva Makes Waves in Wearables"). When the radios are idle, the core can simultaneously run the software for all of the voice codecs, for positioning, and for sensor functions. Such a design can integrate with the radio on a single chip when manufactured in RF-CMOS technologies such as 65nm, 55nm, or 40nm, which the company expects will enable smartwatch battery life of a week or more.

NB-IoT designs typically employ a CPU with DSP extensions, such as ARM's Cortex-M4, to run the protocol stack and baseband functions. The X1 is a multipurpose core with DSP capabilities optimized for the new low-speed standard, but it can also deliver 3.3 CoreMarks per megahertz—just 0.1 less than the ARM CPU—on general-purpose code, thus providing a complete replacement for the ARM core. Along with the Ceva software libraries, the X1 offers a complete NB-IoT package. ♦