CEVA®
The DSP Powerhouse

CEVA-XC4500

THE WORLD'S FIRST VECTOR FLOATING-POINT DSP FOR WIRELESS INFRASTRUCTURE APPLICATIONS

Overview

The CEVA-XC4500 DSP core is optimized for high-performance wireless infrastructure equipment. It features a combination of VLIW (Very Long Instruction Word) and vector engines that enhance typical DSP capabilities with advanced scalar and floating-point vector processing.

Based on the architecture of the CEVA-XC4000 DSP family, the CEVA-XC4500 DSP core has an advanced vector-processing unit supporting both fixed-point and floating-point instruction sets. Built-in support for traffic management and dynamic scheduling provides efficient data processing within base stations, remote radio heads, and backhaul equipment. Supported by full hardware cache coherency, multiple cores can be deployed to scale the amount of traffic to be handled, from picocells to macrocells to Cloud-RAN, with no software overhead. With its innovative programmable approach, the CEVA-XC4500 offers the high flexibility needed to support a large number of wireless standards on a single programmable platform, thereby significantly reducing development cost and time-to-market.

The fourth generation of the CEVA-XC family, the CEVA-XC4500 is optimized for the increasingly advanced applications that implement the complex new protocols required to deliver high-speed data and increased capacity on an evolving wireless network.

The Future of Wireless Infrastructure

According to a Cisco VNI Mobile report from February 2014, global mobile data traffic grew 81 percent in 2013, and will continue to grow at a CAGR of 81 percent from 2013 to 2018, reaching a 11-fold increase over 2013 by 2018. Today's 4G technologies (LTE, HSPA+, etc.) support significantly higher data rates than previous generation standards, but 4G data rates do not even come close to having the ability to meet the expected data traffic demand over the next few years.

In the past, wireless infrastructure was largely homogeneous, consisting of similar-sized cells and base stations. The future build-out, by contrast, will move in two different directions: a heterogeneous mix of different-sized cells (the HetNet) and Cloud-RAN, through which a large number of remote radio heads feed into a very large central base station. This variety of equipment creates a need for a scalable architecture so that a single, consistent platform can serve the requirements of all of these systems using the same software, providing scalability and efficiency.

The CEVA-XC4500 Platform

The CEVA-XC4500 platform, based on the CEVA-XC4000 family, is the fourth generation of the CEVA-XC DSP architecture. It leverages the widely-licensed, industry-proven CEVA-XC processor architecture and is backward compatible with previous generations. The scalable architectural framework of the CEVA-XC4000 family defines a series of communication DSPs optimized for numerous wireless standards, thereby ensuring cost and power efficient software defined radio (SDR) implementation in both wireless terminal and infrastructure applications.

Such an infrastructure platform needs to meet extreme and sometimes contradicting challenges, including:

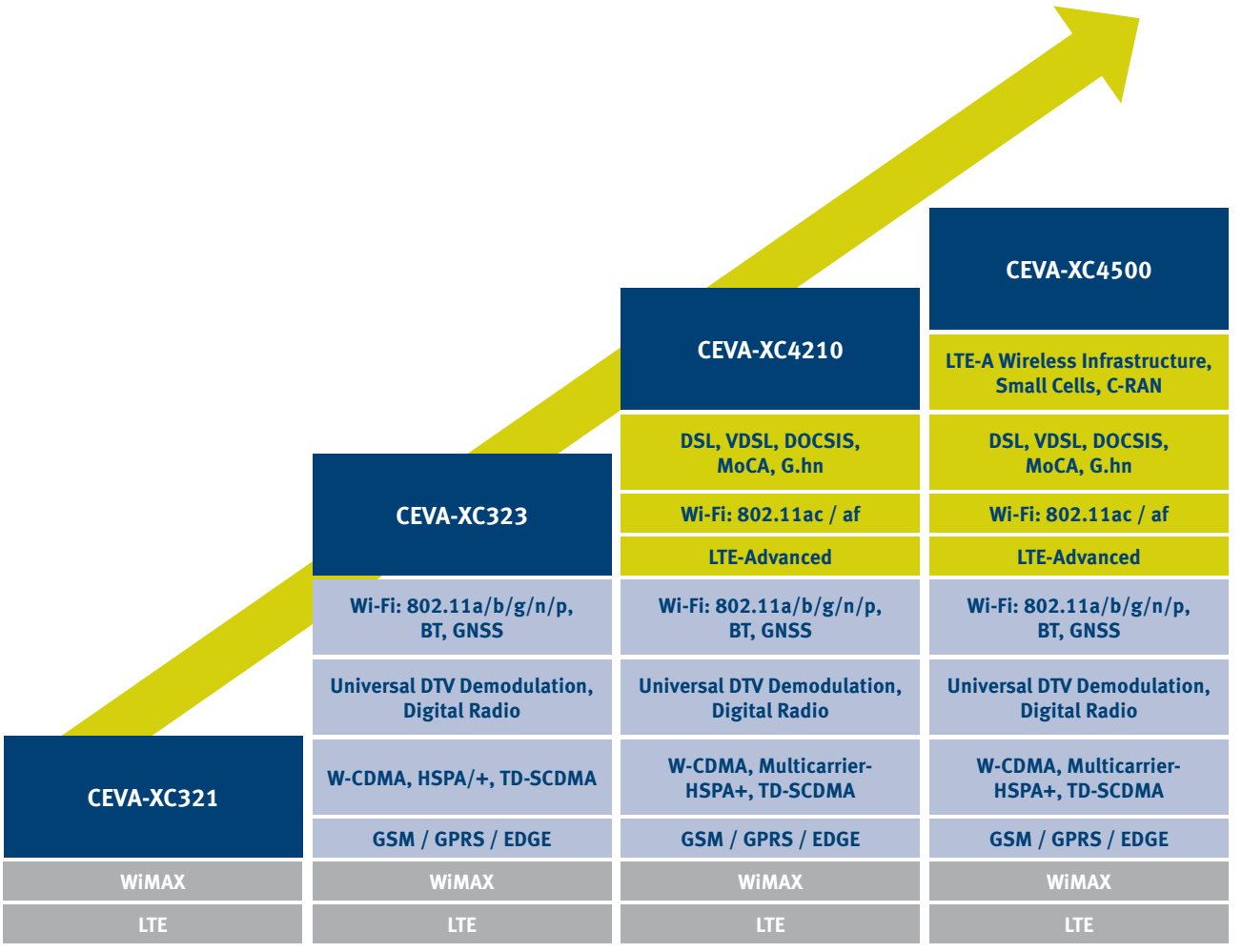
- High Performance: Meeting the requirements of advanced communications: LTE-A, multi-carrier HSPA+, etc. on the radio receiving end
- Fast Time-To-Market: Enabling easy adaptation to a variety of cell sizes using various evolving radio technologies
- Low Power Consumption: Minimizing the need for cooling and power delivery to remote sites and Small Cells
- High Flexibility: Offering optimal performance-power/cost balance for different standards and types of infrastructure equipment
- High Modem Quality: Support for challenging receiver algorithms, including high dimension MIMO, high spectral efficiency, etc.

Features

- A cache-coherent processor that allows scaling for a wide variety of wireless infrastructure systems
- Fully programmable DSP architecture incorporating a unique mix of VLIW and vector capabilities via a combination of computational units:
  - Vector Communication Units – fixed point and floating point
  - General Computation Unit
- High-performance architecture
  - Over 1.3GHz on a 28nm process
  - 40 GFLOPs
  - Variable 16/32-bit instructions
  - 13-stage pipeline
- Complemented with CEVA-Toolbox, the industry's most advanced software development environment:
  - Advanced IDE
  - Optimizing C compiler with vector types support
  - Cycle-accurate simulation and graphical profiling of the entire DSP sub-system
  - Advanced debug and profiling capabilities in emulation mode using an FPGA or silicon chip
  - Macro assembler, linker, and GUI debugger
  - RTOS
  - Smooth migration path from off the-shelf ASSPs
  - MATLAB bi-directional connectivity
- Complete set of optimized communication libraries covering the transceivers for a wide range of wireless standards, including LTE, TD-LTE, HSPA+, LTE-A, TD-SCDMA, and more.
- Advanced multi-core support includes snooping, message queues, fast interconnect, queue manager, buffer managers, and more.

Benefits

- Saves significant design time and effort by allowing designs to be scaled for any portion of the HetNet or Cloud-RAN with minimal rework
- Optimized for high-speed handling of data packets to be delivered to and from the radio
- Supports critical service provider features like quality of service (QoS)
- Provides an extensive instruction set optimized for a wide range of communication standards to enable software-defined modem implementation:
- Smooth C-level software development with a special advanced Software Development Kit (SDK),accelerating time-to-market
- System scalability for different use cases and easy integration into customer SoCs



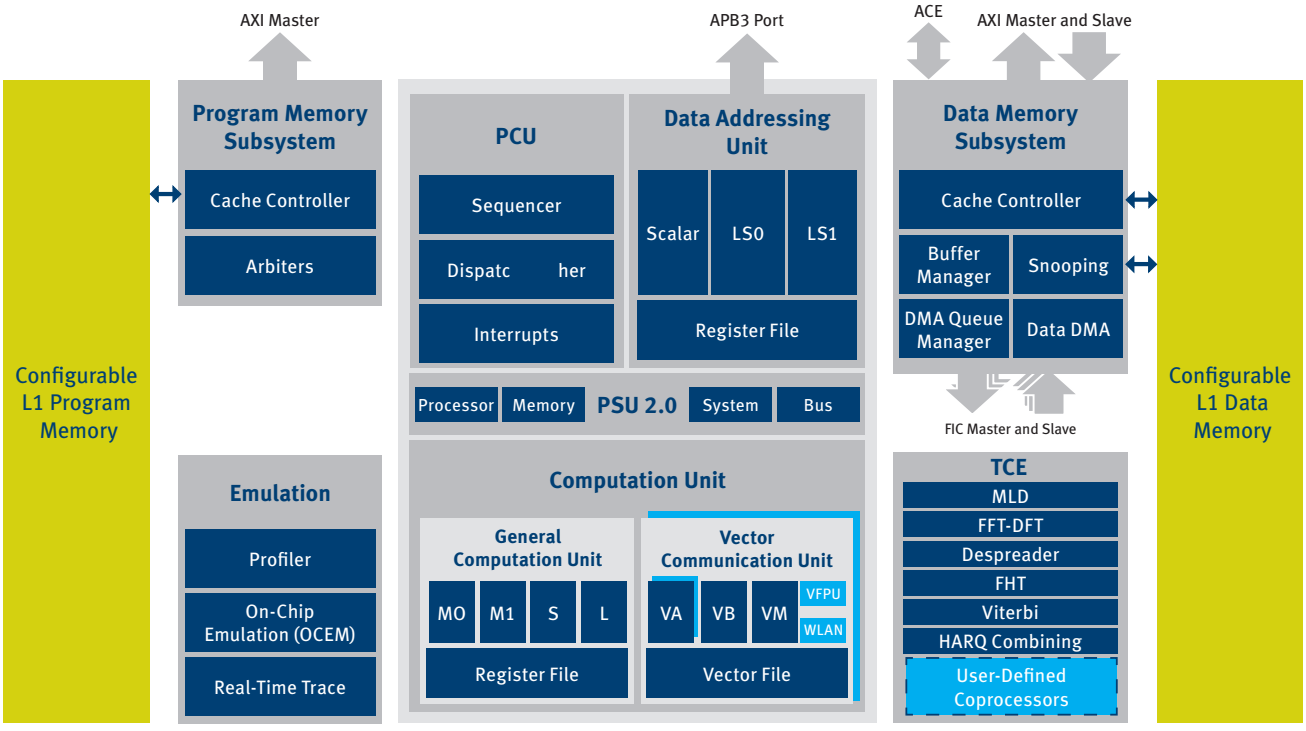
CEVA-XC4500 Modem Platform

The CEVA-XC4500 implements an advanced wireless data packet processing engine. Multiple cores can be easily added to scale up or down the supported packet rate, number of users and cell type. Configuring the cores as symmetric clusters allows software to be written independently of the number of cores in any specific system. Advanced scheduling and queue management functions allow both for run-to-completion data plane (fast-path) functions as well as implementation of select management or slow-path functions that might benefit from being handled in the DSP instead of being pushed to a hardware accelerator.

The base station radio is supported by additional features, including high-dimension complex mathematics solutions with a new multiple-input multiple-output (MIMO) instruction set architecture (ISA) for QR/Cholesky decomposition; advanced mechanisms to match maximum likelihood (ML) solutions in high MIMO dimensions, and the ability to support up to 16 division, square root, and inverse square root operations per cycle. An orthogonal register file provides up to 32 vector registers with either 256-bit or 320-bit wide access, minimizing register transfers and memory accesses, thereby ensuring high system performance and low power consumption.
The CEVA-XC4500 is equipped with a second-generation power scaling unit (PSU 2.0). The new PSU 2.0 supports advanced power management techniques addressing the core, system-level control plane, buses, memories, tightly-coupled extensions (TCEs), and more. The PSU manages both dynamic and leakage power and provides an enhanced power-optimized pipeline with low-level module isolation and optimized vector element utilization.

The use of TCEs allows higher performance while simultaneously reducing power consumption. The TCEs augment the CEVA-XC4500 cores with a selection of coprocessor units, thereby providing the most efficient, lowest-power implementations of demanding transceiver algorithms. Supported TCEs include a programmable multidimensional ML decoder (MLD), fast and discrete Fourier transforms, a fully programmable de-spreader and FHT solution that addresses all 3G standards, Viterbi encoding, and HARQ combining.

Furthermore, the TCE coprocessor interface allows customers to use their existing proprietary IP block as a dedicated coprocessor. The TCEs can run in parallel to the main DSP functions, reducing the burden on the main DSP core. By offloading the main core, its frequency can be lowered, thereby further minimizing power consumption.



CEVA-XC4500 block diagram

The CEVA-XC4500 provides uncompromising modem quality with less than 0.3dB loss for the entire LTE-A receiver chain. The CEVA-XC4500 offers enhanced precision using several mechanisms. including support for high precision 16x32 and 32x32 arithmetic, floating-point and more.

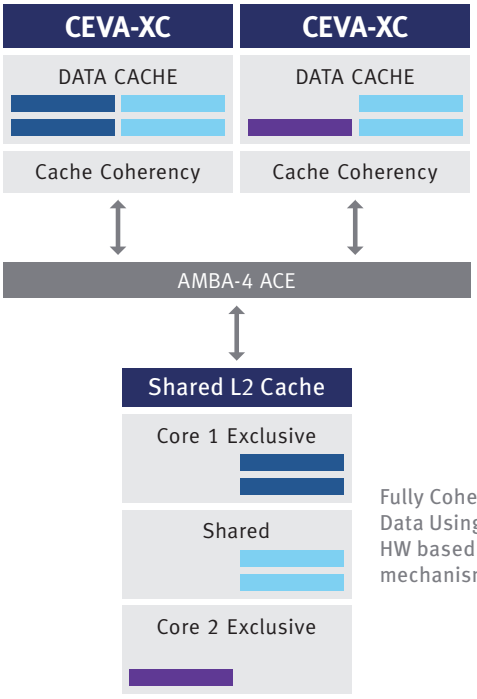
System-level design is facilitated by a new fast interconnect (FIC) system interface that complements existing AXI master and slave ports and enables high-bandwidth, low-latency connectivity between multiple cores and hardware accelerators. The FIC supports a user-configurable number of master and slave read/write ports, coupled with a configurable bus width of up to 1024 bits, thereby providing an overall bandwidth of up to 1.5 terabytes per second. A DMA queue manager facilitates data traffic management, DSP offloading, and prioritized scheduling for guaranteed Quality-of-Service (QoS). An automated buffer manager enables low latency without software intervention, resulting in lower memory consumption.

Cache coherency

Effective, efficient cache coherency is a primary requirement for any multicore system. Software implementations are possible, but they rob the main processes of critical clock cycles and memory resources. By implementing a hardware cache coherency system based on the ARM ACE protocol, the CEVA-XC4500 provides full cache coherency with no software overhead.

External memory can be logically mapped into regions, some of which will be shared between cores, others being private to a core. Coherency snooping will be applied only to data that resides in shared memory regions, improving performance and lowering power consumption.

In addition, a hardware implementation removes coherency from software, allowing coherency operations to take place in the background. This decouples coherency considerations from the application programs, making the programs easier to develop and scale across a variety of platforms, whether single- or multi-core.

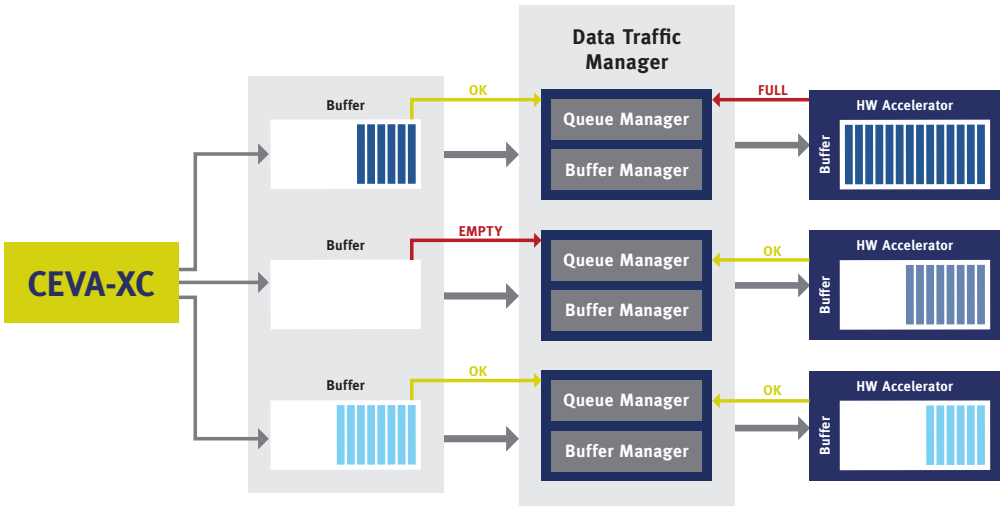


Fully Coherent Shared L2 Data Using AMBA-4 ACE HW based coherency mechanism

Data Traffic Management

Wireless traffic will consist of packets from a large number of calls, data sessions, or flows, each with its own processing requirements. Some packets will have higher priority due to QoS, time sensitivity, or management status. Others may require more processing. A single queue for all such packets runs the significant risk that one packet with lower priority requiring more processing will block higher-priority packets.

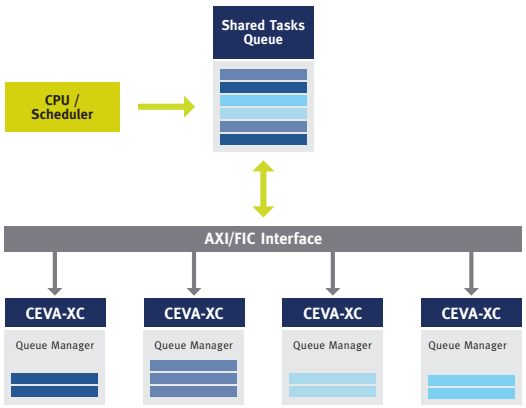
The CEVA-XC4500 allows multiple independent queues to be maintained, each with its own priority and status. A built-in data traffic manager automatically takes priority, buffer status, and processing status into account to ensure both high-priority packets are addressed first and blocked flows don't impede the further processing of other unblocked flows. This allows processing resources to be shared between different cores while minimizing resource idle time and ensuring that high-priority packets get processed first.



Dynamic Task Scheduling

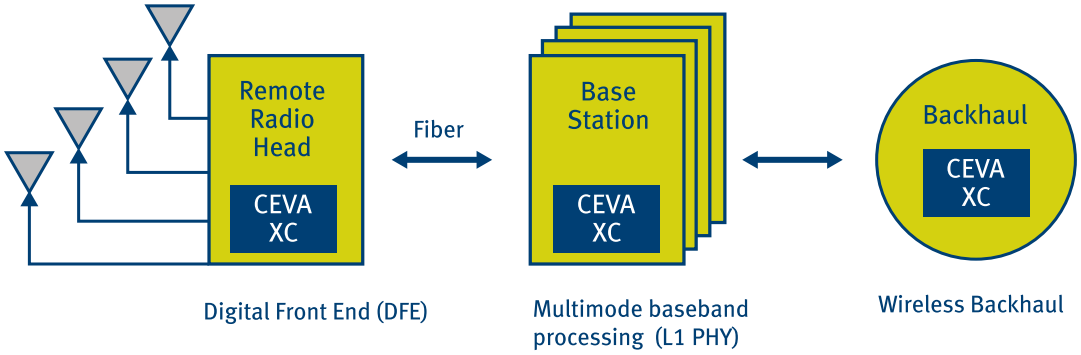
An effective wireless packet processor must be able to adapt to real-time changes in traffic patterns. A homogeneous cluster of DSP cores makes this possible through the dynamic assignment of tasks to cores and the subsequent assignment of work to each of those cores.

Tasks can execute efficiently based on tight run-to-completion code. If the load for a given task becomes too high, then cores can be reassigned to balance the load more effectively. The CEVA-XC4500's scheduler manages this using algorithms that can be implemented when the system first loads.



CEVA-XC4500 Applications

CEVA-XC4500 applications include, but are not limited to:



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