PRODUCT BRIEF

CEVA®
The DSP Powerhouse

CEVA-XC323

HIGH-PERFORMANCE VECTOR DSP FOR SOFTWARE DEFINED RADIO INFRASTRUCTURE APPLICATIONS

Up to 4x performance improvement over existing 4G wireless infrastructure DSP

FEATURES

- Optimized for Wireless Infrastructure
  - Enables software-defined modem design with minimum hardware requirements
  - Extensive support for wireless infrastructure applications
- Fully Scalable
  - Supports a homogeneous multi-core system design
  - High flexibility with optimal performance-cost tradeoffs
  - Applicable from small femtocells to macro base-station applications
- Easy Software Development
  - Optimizing toolchain includes C Compiler with dedicated support for Vector Processors
  - Cycle-accurate simulation and profiling of the entire DSP subsystem
  - Access to a complete set of DSP and communication libraries
- Seamless Migration from previous-generation infrastructure DSPs
  - Easy reuse of TI C6x optimized source code

BENEFITS

- High-performance satisfies the extreme DSP requirements of 4G applications
- Offers dramatic cost reduction compared to today's systems
- Ultra-low power consumption allows use in a wide variety of target environments
- Comprehensive support for system connectivity ensures easy integration into multi-core SoCs
- C-level software development and a complete set of DSP and communication libraries reduce risk and time-to-market
- Ease of migrating existing and legacy designs from expensive off-the-shelf devices facilitates reuse of investment
- A scalable processor applicable to different infrastructure devices from small femtocells up to macro base-stations
- Accompanied by CEVA-XCnet partners for a complete 3G/4G PHY solution

The Wireless Network is Changing

The wireless industry is poised on the brink of a cellular network inflection point. The combination of a continuous growth in the number of users and an exponential growth in the amount of wireless data is resulting in major bottlenecks in the existing infrastructure topology.

Type	Typical Range	Numbers of Users	Data rates: LTE Cat-4
Femtocell	Indoors	8 / 16 / 32	150 Mbps
Picocell	In building / small area	32 / 64	450 Mbps
Microcell	0.1Km - 1Km	> 100	1.5 Gbps
Macrocell	1Km - 70Km	> 100	4.5 Gbps

Simply increasing the size of base station cells is not the answer because this requires a huge investment coupled with power consumption considerations and low spectrum efficiency. The alternative is to move to a heterogeneous hierarchical network involving femtocells, picocells, microcells, and macrocells. In particular, analysts forecast mass-market adoption of femtocells and picocells, both of which have a high sensitivity to power consumption and silicon cost.

The Solution is the CEVA-XC323

The CEVA-XC323 is a highly powerful next-generation communication DSP core that fully addresses today's requirements for extreme processing, flexibility, scalability, and ultra-low power consumption. Optimized for the specific needs of wireless infrastructures, the CEVA-XC323 runs the majority of the PHY layer in software, thereby eliminating the need for various hardware accelerators found in existing solutions. With its fully programmable architecture, the CEVA-XC323 handles the full 4G transceiver path in software and also supports both legacy and next generation wireless standards such as WCDMA, HSPA+, WiMAX, LTE and LTE-A. The CEVA-XC323 also provides extensive support for the eNodeB data plane, support for multi-user eNodeB applications, and can be complemented with CEVA-XCnet software to provide a complete 3G/4G PHY solution.

The CEVA-XC323 leverages the architectural efficiency and mature software development environment of the existing CEVA-X family of DSP cores, which have shipped in more than 100 million devices to date. Building on this success, the CEVA-XC323 boasts a wealth of features, including support for AXI system busses, an integrated Power Scaling Unit (PSU), and a seamless migration path from TI infrastructure DSP chips.

High Performance, Highly-Scalable Architecture

The CEVA-XC323 core combines typical DSP capabilities with advanced vector processing. The result is 8-way VLIW, 512-bit SIMD, 32 MAC operations per cycle, and native support for complex arithmetic. Also, full software compatibility with the CEVA-X enables strong support for non-vectorized operations. Optimized for use in wireless infrastructures, the CEVA-XC323 provides extensive instruction sets covering all PHY requirements, including DFT, high-precision FFT, channel estimation, MIMO detectors, interleaver/de-interleaver and inherent support for Viterbi decoding.

The CEVA-XC323 is highly scalable for use in a wide range of infrastructure devices, from small femtocells and picocells all the way to microcells and macrocells. It offers homogeneous multi-core system design capability that includes wide Advanced eXtensible Interface (AXI) busses for massive data transfers; a snooping mechanism to detect external device accesses to internal memory buffers; message queues allowing synchronization and easy system control; exclusive access allowing atomic access to external memories, thereby enabling data sharing between multiple cores; and external debug interfaces allowing cross-triggering. The CEVA-XC323 is also extensible to implement customer-specific IP in software. The result is to provide high flexibility and support optimal performance-cost tradeoffs.

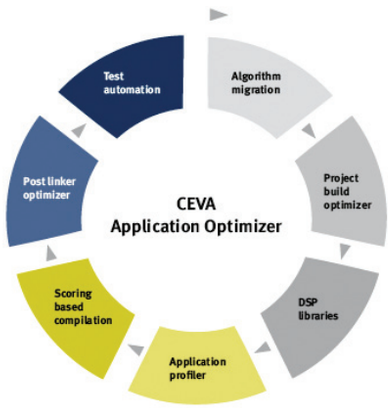
Energy Efficient

The CEVA-XC323 DSP core offers significant energy savings for both battery-operated and stationary devices – a critical factor in an increasingly energy-conscious world. The CEVA-XC323 includes an integrated Power Scaling Unit (PSU), which provides advanced power management for both dynamic and leakage power.

The core supports multiple voltage domains associated with the main functional units, such as the DSP logic, the instruction and data memories, and so forth. The core also supports multiple operational modes ranging from full operation, to debug bypass, to memory retention, to complete power shut-off (PSO). Furthermore, the AXI full duplex buses offer low-power features, such as ability to shut down when no data traffic is present.

Effortless Software Development

The ability to program in C is essential for reducing development time and ensuring easy portability to future platforms. The CEVA-XC323 DSP was designed together with its optimizing C-compiler to ensure optimal utilization of the processor capabilities. CEVA-XC323's compiler supports the CEVA Vec-C™ language extensions for vector processors, enabling the entire architecture to be programmed in C-level. The processor is supported by a complete software development, debug, and optimization environment in the form of the CEVA-Toolbox™.



CEVA-Toolbox is an advanced Integrated Development Environment (IDE), which includes a powerful compiler that facilitates software development without the need for users to master architecture-specific details. An integrated simulator provides accurate and efficient debug capabilities of the entire system including the memory sub-systems. In addition, CEVA-Toolbox includes libraries, a graphical debugger, and a complete optimization tool chain named CEVA Application Optimizer. The Application Optimizer enables automatic and manual optimization applied in the C source code.

Seamless Migration from TI C6x DSPs

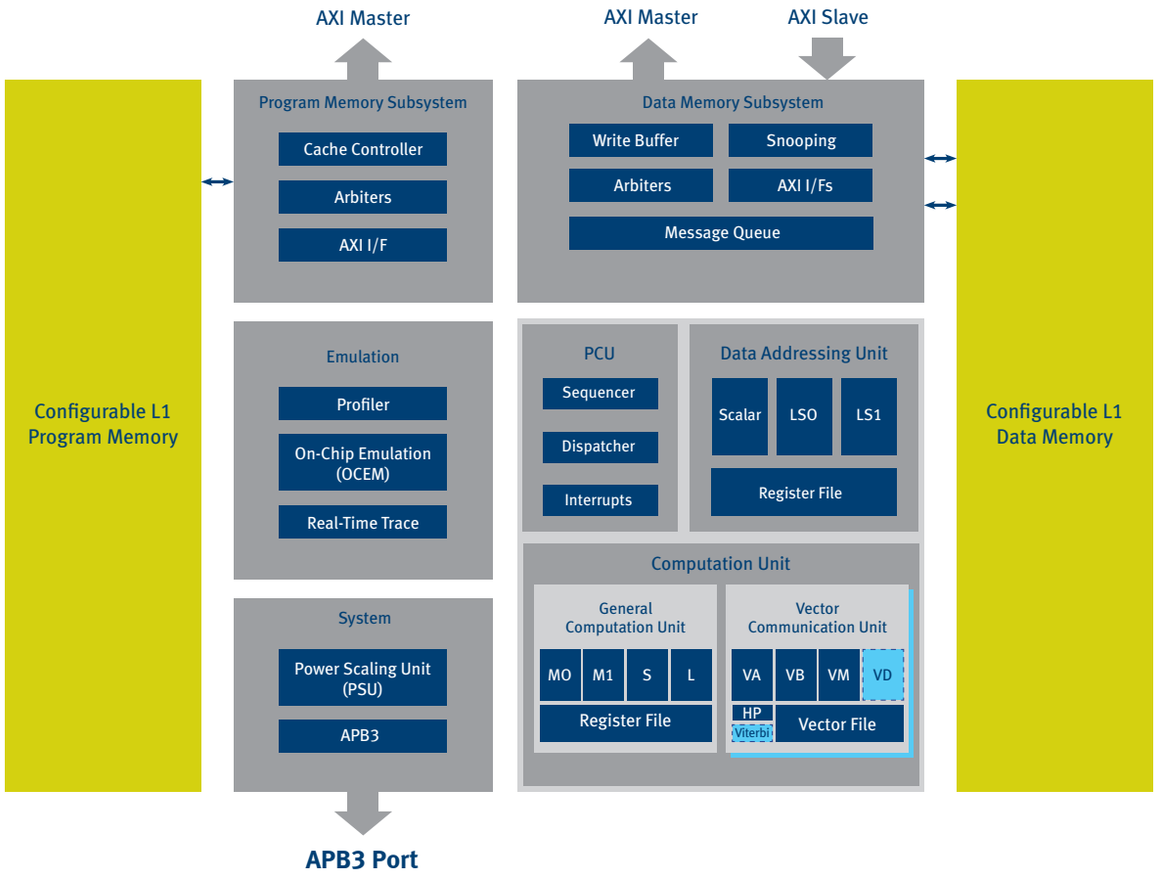
With the availability of next-generation DSP IP architectures – such as the CEVA-XC323 – the design world is transitioning from using off-the-shelf DSP chips to incorporating DSP cores in custom system-on-chips (SoCs).

The CEVA-XC323 supports easy software migration from off-the-shelf DSP chips to incorporating DSP cores into customer SoC designs. The combination of extended compiler support for legacy DSP software with similar system architecture enables licensees to quickly and efficiently migrate legacy code while ensuring up to 4x DSP performance levels at a significantly lower price point.

State-of-the-Art Prototyping Platform

Today's increasingly complex SoC designs require development teams to have the ability to verify the design before taping out the actual silicon. CEVA offers a complete hardware-based development platform including development boards that assist system and software designers in validating their SoC application designs.

Advances in FPGA technology and the increase of FPGA capacity have made these devices a valuable tool for SoC prototyping and verification. CEVA provides dedicated ASIC to FPGA synthesis tools and development boards that allow users to take "black box" instantiations of CEVA DSP cores and use them in FPGA-based prototyping systems. The FPGA-based hardware platform interfaces to a host PC via a JBox interface, thereby providing full application control including all required functionalities, such as breakpoints, real-time tracing, profiling, etc.



CEVA-XC323 - Block Diagram

About CEVA's DSP Cores

CEVA is a leading licensor of programmable Digital Signal Processor (DSP) cores for use in consumer electronics, home entertainment, mobile handset, portable multimedia, and communications applications.

CEVA's DSP cores are licensed to leading electronics companies as Intellectual Property (IP). These companies use CEVA's IP cores in their Application-Specific Integrated Circuit (ASIC), Application-Specific Standard Product (ASSP), and System on Chip (SoC) devices.

CEVA's product line includes a wide variety of DSP cores. Each core delivers a different balance of performance, power dissipation, and cost, thereby allowing users to select the optimal core for the target application requirements.

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